



# TECH *report*

EDITION NINE - JULY 2010

Accelerating the next technology revolution



In this edition:

SEMICON West 2010

# Collaboration Across the Industry Supply Chain Making EUV Lithography a Reality

*Dan Armbrust, President and CEO*



Implementation of the game-changing technology of extreme ultraviolet lithography (EUVL) is about to happen – that’s the message from Lithography Director Bryan Rice in this edition’s quarterly interview. This encouraging forecast comes after more than a year of hard work by Rice, Vice President of Advanced Technology John Warlaumont, Litho Associate Director Stefan Wurm, and others to engineer one of the most innovative and challenging technology collaborations in our industry..

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**Our lithography team’s accomplishment illustrates that today’s challenges require collaboration across the supply chain – especially in technologies that cost too much for any single company to reasonably afford.**

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But systemic collaboration isn’t easy. Participants must become financial stakeholders while sharing sufficient specifics of their roadmaps and technical insights for the common good. This behavior doesn’t occur naturally in our intensely competitive industry, and so it takes an organization such as SEMATECH to help form a consensus to ensure that the right technology becomes available at the right time. How this was done for EUVL is worth exploring.

For several years, the SEMATECH Lithography program had been focusing on overall issues in resist development, mask defectivity, and patterning to help prepare EUVL for pilot manufacturing in 2013. But within the industry, the pace of scanner development and the lack of effective metrology were creating doubts that EUVL would arrive. Most

leading edge manufacturers were working on alternatives, such as double exposure/double patterning and various computational approaches, even as they acknowledged that these departures would not offer the projected cost and scaling benefits of EUVL.

Recognizing that a large-scale rejection of EUVL would negatively impact the industry, SEMATECH decided in early 2009 to work to remove the remaining roadblocks to the technology. It was a natural role for us, since we already were working on the most critical aspects of EUVL, including low-defect mask blanks, advanced resists, and mask infrastructure.

The Litho team led by Warlaumont, Rice and Wurm scheduled one-on-one meetings with EUVL stakeholders around the world. Among them were chip-makers, merchant mask shops, mask blank suppliers, metrology tool makers, and scanner manufacturers. To this diverse set of companies Litho’s basic message was the same: EUVL is not a way for companies to gain competitive advantage over one another – it’s a technology that must be addressed collaboratively across the entire supply chain, or it won’t be available to anyone.

It wasn’t an easy process. Some companies did not have EUVL on their technology roadmap, and had to be convinced it belonged there. Others hung back out of fear that taking a position would reveal their technology introduction roadmaps. Several stakeholders were uncomfortable with the need to put their cards on the table.

But our team persevered, and by SEMICON West 2009 SEMATECH convened a supply chain meeting where manufacturers and suppliers actually described how their business strategies coincided with EUVL. As Rice puts it: “After

that meeting, EUVL was on everyone's roadmap. That was key to really moving forward with the technology."

Subsequently, SEMATECH continued meeting one-on-one with stakeholders to clarify ideas and positions, and in October brought the industry together once again at the 2009 International EUVL Symposium in Prague, Czech Republic. There, all of the invited companies gave presentations on their status and plans in EUVL. "It wasn't until Prague that we had the first open technical discussion where people finally said what they were thinking," Rice noted. "In that meeting we learned how to really communicate with each other, and where the true technology gaps were."

A troublesome gap was the lack of EUV-ready mask blanks, and the metrology tools necessary to measure defects on them, leading a subset of chip makers and suppliers to begin planning a new collaboration in that direction – and resulting in the launch earlier this year of our EUVL Mask Infrastructure (EMI) Partnership at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany. Already with seven members, the EMI Partnership is open to mask and chip-makers, mask blank suppliers, regional governments and other consortia.

Another boost came when ASML received orders for its pre production, and subsequently, its manufacturing capable EUV scanners – creating the investment critical mass to ensure that the tools would be built. Presentations and surveys at the SEMATECH Litho Forum in May further confirmed that the industry requires the cost and technology benefits EUVL will provide, and considers EUVL the most feasible next-generation lithography technology. These wins, combined with other incremental victories, have persuaded most

industry players that EUVL is real and will be used for high-volume production within the next few years.

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**SEMATECH's and the industry's experience in driving EUVL to manufacturing maturity shows that even die-hard competitors can go outside customary business practices and collaborate on a major technology introduction, once several key elements – technical readiness, consensus on timetable, willingness to invest, and a new collaborative model – converge.**

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I believe the shared risk model that emerged from our EUVL collaboration will be repeated in other emerging technologies, such as 3D through-silicon via (TSV) interconnect. With today's industry structure, it is inevitable that major technology transitions will have to be addressed by the full supply chain in unaccustomed collaborations. SEMATECH's role will be to help organize and consolidate competing views, identify top challenges, and champion programs to overcome the technical and financial roadblocks that are critical to our industry's future.

# SEMATECH to Highlight Leading-Edge Research in Technology and Manufacturing at SEMICON West 2010

*Presentations and public workshops feature 3D interconnects, advanced materials, and manufacturing methods*

SEMATECH and International SEMATECH Manufacturing Initiative (ISMI) will highlight current research through a wide range of lectures and workshop sessions from July 13-15, in conjunction with SEMICON West 2010 in San Francisco, CA.

SEMATECH and ISMI experts will report their latest advances in new materials and device structures, next-generation metrology, and equipment and fab productivity, with a special focus on addressing key opportunities and challenges in 3D interconnect technology.

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**“Our goal is to promote innovative and practical solutions for continued scaling of semiconductor technologies that can easily be incorporated in to real-world manufacturing environments,”** said Dan Armbrust, president and CEO of SEMATECH. **“Through various presentations and workshops we look forward to sharing our technical knowledge and best practices, exploring the promise of 3D interconnects, and introducing new manufacturing concepts to help drive our industry forward.”**

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## July 12, 2010

**ISMI Equipment Energy Workshop - Overspecification**  
Equipment suppliers and end users will meet to address the issue of overspecification of utility capacity for semiconductor process tools.

**8am, Marriott Marquis**

**ISMI Equipment Energy Workshop – Standardized Communication Protocol for Idle Mode**

Equipment suppliers will discuss the viability of a standard communications interface protocol between the main tool and support equipment such as roughing vacuum pumps and point of use abatement devices.

**1pm, Marriott Marquis**

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## July 13, 2010

**OEM-focused Dry Etch Process Equipment Workshop**

Part of the ISMI Installed-base Equipment Series

**8am, Marriott Marquis**

**Stress Management for 3D ICs using Through Silicon Vias**

Hosted by SEMATECH, in collaboration with Fraunhofer IZFP, the second workshop on Stress Management for 3D ICs using Through Silicon Vias will discuss DFM-like approaches for managing stress, including required material properties, measurement techniques and corresponding simulation use modes.

**9am, Grand Hyatt**

### **3D Interconnect Challenges and Need for Standards Workshop**

Co-sponsored by SEMI and SEMATECH, this workshop will provide the vision and progress to date on 3D TSV integration, solicit areas of concern, and identify the areas of variance between existing solutions and proposed/anticipated solutions.

**1pm, Marriott Marquis**

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## **July 14, 2010**

### **Equipment Productivity Workshop on Dry Etch Chambers**

Part of the ISMI Installed-base Equipment Series

**8am, Marriott Marquis**

### **Paul Kirsch, SEMATECH's director of Front End Processes**

"Metal Oxide RRAM as a Future Non-Volatile Memory Technology,"

**11am, SEMICON West TechXPOT Stage**  
**- North Hall of Moscone Center**

### **Dilip Patel, ISMI's Metrology program manager**

"Measuring the Nanoscale: Metrology Challenges in Manufacturing,"

**12pm, SEMICON West TechXPOT Stage**  
**- North Hall of Moscone Center**

### **Bryan Rice, SEMATECH's director of Lithography**

Moderator of the Advanced Lithography TechXPOT session

**2pm - 4.30pm, SEMICON West TechXPOT Stage**  
**- North Hall of Moscone Center**

### **SEMATECH's 3D Metrology Workshop**

Equipment suppliers will share their plans on how new and existing wafer metrology technologies can be used, modified, or enhanced to measure and improve 3D interconnect processes.

**1pm, Marriott Marquis**

### **ISMI's e-Manufacturing Workshop**

Co-organized with SEMI, ISMI's e-Manufacturing Workshop will focus on the Equipment Data Acquisition interface (Interface A). e-Manufacturing enabling implementation strategies on the Interface A requirements, including the next freeze level, will be presented to an audience of chip-makers, equipment companies and software suppliers.

**1pm, Marriott Marquis**

### **SEMICON West Reception**

SEMATECH invites you to join our executive and technical staff at our annual reception at SEMICON West. Stop by to socialize and network with industry friends and colleagues - we hope to see you there!

**5.30pm - 7.30pm, Golden Gate Hall - Marriott Marquis**

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## **July 15, 2010**

### **OEM-focused Dry Etch Process Equipment Workshop**

Part of the ISMI Installed-base Equipment Series

**8am, Marriott Marquis**

### **ISMI's Product and Equipment Time Metrics Workshop**

Co-organized with SEMI, ISMI's Product and Equipment Time Metrics Workshop will provide a forum to introduce the concept of "Product and Equipment Time Metrics" to the semiconductor industry. Participants will gain an understanding of the definition and use of the time metrics concepts as an alternative method for identifying, measuring, and improving factory and equipment productivity.

**1pm, Marriott Marquis**

# Qualcomm and SEMATECH Sign Collaborative Agreement

*Collaboration to Broaden Industry Alignment on Key Roadmap Challenges*

Qualcomm Incorporated (Nasdaq: QCOM), a leading developer and innovator of advanced wireless technologies, products and services, has announced that Qualcomm has entered into a collaborative agreement with SEMATECH to advance CMOS scaling and assess new technologies.

As the first integrated, fabless chip manufacturer to join SEMATECH, Qualcomm plans to participate in a high-level engagement to assess the feasibility of technologies that are designed to extend Moore's Law.

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**“We are pleased to welcome Qualcomm to SEMATECH and we look forward to gaining important insights from Qualcomm, given their leadership in the fabless community and mobile application solutions, on how we can shape our advanced technology programs to meet the industry's future needs,” said Dan Armbrust, president and CEO of SEMATECH. “This new collaborative effort broadens the scope of participation in SEMATECH, and underscores our commitment to bring all sectors of the industry together in assessing technology options, creating standards, building early infrastructure and charting overall industry direction.”**

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“Qualcomm has a long history of working with various industry partners to specify and drive the next generations of process technology,” said Jim Clifford, senior vice president and general manager of Qualcomm CDMA Technologies. “SEMATECH’s strong affiliation with chip manufacturers and suppliers, universities and research institutions around the world, coupled with its R&D capabilities and technical knowledge, offer an excellent opportunity to enhance our participation in the industry’s technology agenda and help shape the industry’s direction.”

This collaboration with Qualcomm is one facet of SEMATECH’s strategic initiative to develop new opportunities for creative cooperation across the semiconductor ecosystem so as to address the industry’s technical and business challenges and reduce the cost and risk of major technology transitions. SEMATECH has expanded its programs participation to include fabless companies, as well as chipmakers and equipment and materials manufacturers, to drive industry consensus and provide cost-effective solutions.



New Members

## Edwards Vacuum Joins ISMI's ESH Technology Center

*Partnership to advance green semiconductor operations and processes for sustainable semiconductor manufacturing*

Edwards Limited, a leading global supplier of vacuum and abatement equipment and services, has joined ISMI's Environment, Safety and Health (ESH) Technology Center.

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**Within the Center, Edwards will collaborate with hundreds of ESH experts and consultants from around the world to develop data-driven solutions in areas such as energy and resource conservation, chemical management, and industry response to climate change.**

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"We're pleased to welcome one of the leading manufacturers of vacuum equipment to ISMI's ESH Center," said Ron Remke, ISMI's ESH program manager and head of the Center. "At the Center we are working through all levels of the supply chain to address the industry's need for sustainability, productivity, and cost-effectiveness. We look forward to working closely with Edwards in an effort to keep our industry's manufacturing businesses productive, profitable, and sustainable, while significantly reducing the environmental footprint of manufacturing operations."

Scott Balaguer, General Manager, America's Edwards stated, "We are very excited to become a member of ISMI, and to participate in the ESH program. We have always made it a priority to minimize the environmental impact of our products, which has become even more important with the recent increase in environmental regulations worldwide. For instance, our pumps incorporate the ability to operate in several process specific green modes, reducing power



consumption between 20 and 99 percent," Balaguer adds, "The data we will derive from this partnership will help us develop new environmentally-friendly capabilities for our products."

The SEMATECH and ISMI ESH program has been pursuing energy and resource conservation for over 15 years and has published several dozen reports and presentations which collectively document best practices for energy and resource conservation. For example, ISMI was successful in providing proven process data (etch rate, uniformity, particles) to enable member companies to implement vacuum pump idle mode savings in their own facilities with confidence.

In 2009, ISMI launched its ESH Technology Center to further address the energy and resource conservation needs of the semiconductor industry. The center is the industry's first global collaborative research effort dedicated to finding and implementing green technologies that reduce energy consumption, lower costs, and promote greater productivity in manufacturing. Participating companies share ideas and resources, while directing, evaluating, and refreshing the program portfolio.

# JSR Moves to Join SEMATECH's Resist Center

JSR Corporation, an advanced materials supplier to chip-makers and others, and its US operation, JSR Micro, Inc., announced today that JSR has signed a letter of intent to become the newest member of SEMATECH's Resist Materials and Development Center (RMDC).

JSR will collaborate with SEMATECH engineers on key resist issues in extreme ultraviolet (EUV) lithography. Focus areas will include:

- Working to reduce or eliminate line edge roughness (LER) in lithographic images below 22 nm
- Discovering ultimate resolution of newly formulated photoresists
- Testing various imaging materials for EUV sensitivity

SEMATECH and JSR have partnered previously in several technology development programs, including 300 mm test wafers, low-k films, and advanced resists, including double exposure materials.

"We have a successful history of partnership with SEMATECH and we are excited to continuing that history in the field of EUV", said Hozumi Sato, managing director of JSR Corporation, responsible for the Research and Development. "Combining resources to create to next generation of EUV materials is not only good for JSR and SEMATECH, but will benefit the industry as a whole."



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**"We're looking forward to working with JSR in our mutual effort to develop leading edge resists and materials, and accelerate process availability for EUV pilot line manufacturing," said John Warlaumont, vice president of Advanced Technology at SEMATECH. "Our successful experience in our previous partnerships will contribute greatly to RMDC's effectiveness."**

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At the RMDC, leading resist and materials suppliers participate in focused, cooperative R&D with SEMATECH member companies. Together, the RMDC provides the hardware and research expertise required by materials suppliers and member companies to develop EUV resist processes that meet the stringent resolution, linewidth roughness, and sensitivity specifications needed for EUV insertion at member companies.

# SEMATECH and AZ Electronic Materials to Partner on Critical Issues in EUV Lithography

New Members



AZ Electronic Materials, the global supplier of electronic materials to the semiconductor and flat panel display industries, announced the company has joined SEMATECH's Resist Materials and Development Center (RMDC).

AZ Electronic Materials will collaborate with SEMATECH engineers on crucial resist issues in extreme ultraviolet (EUV) lithography. Specific areas include reduction or elimination of line edge roughness (LER) in images below 22 nm; ultimate resolution of new resists; and testing imaging materials for EUV sensitivity.

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**“Our partnership with AZ Electronic Materials will help strengthen the RMDC’s ability to address critical resist issues in advanced imaging,” said John Warlaumont, vice president of Advanced Technologies at SEMATECH. “This new collaboration illustrates the effectiveness of SEMATECH’s efforts to include a broader range of industry participants in the search for new solutions to our common technology challenges.”**

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“Joining the RMDC provides AZ the opportunity to apply our leading-edge underlayer and top-rinse technologies to the industry efforts to improve EUV performance,” said Geoff Wild, AZ’s CEO. “We expect the use of specialty materials ‘above and below’ the EUV resists will aid in solving some of the current resist processing shortcomings, and we now can test these types of materials at the CNSE.”

At the RMDC, leading resist and materials suppliers participate in focused, cooperative R&D with SEMATECH member companies. Together, the RMDC provides the hardware and research expertise required by materials suppliers and member companies to develop EUV resist processes that meet the stringent resolution, linewidth roughness, and sensitivity specifications needed for EUV insertion at member companies.

# SEMATECH and Lasertec Partner at UAlbany NanoCollege to Develop TSV Solutions for Chip-Stacking Application

Lasertec Corporation of Japan has joined SEMATECH's 3D Interconnect Program at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany, and will partner with SEMATECH to develop robust, cost-effective process metrology technology solutions for readying high-volume via-mid through-silicon via (TSV) manufacturing.

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The collaboration between Lasertec and researchers from SEMATECH's 3D interconnect program will include investigations and comparisons of 3D TSV depth metrology schemes. This work is necessary not only for TSV RIE process control, but also for providing critical feed forward data for wafer thinning and TSV expose processes.

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To facilitate this work, Lasertec will place a 300 mm TSV infrared (IR) etch metrology tool in SEMATECH's 3D R&D Center, providing advanced measurement capabilities that will enable accurate, repeatable TSV depth measurements over a range of TSV dimensions.

## Lasertec

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"We are pleased to welcome Lasertec to the 3D program," said Sitaram Arkalgud, director of SEMATECH's 3D Interconnect Program. "Our common goal is to address the technical challenges of via-mid TSV technology. The metrology expertise of Lasertec combined with the capability of the TSV 300-IR will fill an important gap in our integration scheme. Together, we will provide our Member Companies with a world class TSV depth metrology solution capable of addressing today's needs as well as tomorrow's aggressive dimensions."

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"Lasertec is looking forward to contributing our expertise in the fields of metrology and inspection to further explore innovative metrology capabilities that will make 3D TSVs commercially viable," said Hal Kusunose, CTO of Lasertec. "Our cutting-edge TSV 300-IR tool will allow SEMATECH researchers and SEMATECH's Member Companies to address important metrology challenges of TSV technology."



“The leading-edge research and development that is critical for commercializing innovative TSV technologies will be further enhanced by the addition of Lasertec to CNSE’s Albany NanoTech Complex,” said Richard Brilla, CNSE Vice President for Strategy, Alliances and Consortia. “This new collaboration builds on the SEMATECH-CNSE partnership to support the advanced technology needs of our global corporate partners and the nanoelectronics industry.”

Through-silicon via technology is a method of combining integrated circuits in a vertical stack to enable high functionality and performance with low power consumption in a small footprint. While employing many standard chip processes, TSVs present several new technical and logistical challenges which are being addressed by SEMATECH.

Launched three years ago, SEMATECH’s 3D program was established at CNSE’s Albany NanoTech Complex to deliver robust 300 mm equipment and process technology solutions for high-volume through-silicon via (TSV) manufacturing. To accelerate progress, the program’s engineers have been actively engaging with leading edge equipment and materials suppliers and leveraging their expertise to ready TSV technology. Eventually, 3D interconnects will provide cost-effective ways to integrate diverse CMOS technologies and chips with emerging technologies such as micro and nano electromechanical systems (MEMS, NEMS) and bio-chips.

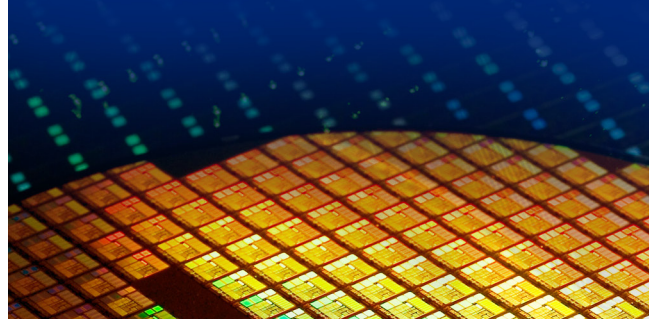
## SEMATECH 3D Interconnect Workshops at SEMICON West

**July 13, 2010**

**Stress Management for 3D ICs  
using Through Silicon Vias  
9am, Grand Hyatt**

**July 14, 2010**

**SEMATECH’s 3D Metrology Workshop  
1pm, Marriott Marquis**



# Interview with Bryan Rice on SEMATECH Lithography



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Bryan Rice, director of SEMATECH's Lithography Program and an Intel assignee, discusses the state of lithography, the importance of R&D alliances, and the development of infrastructure for extreme ultraviolet lithography (EUVL), including SEMATECH's recently launched EUVL Mask Infrastructure (EMI) consortium.

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## **How would you characterize the present state of semiconductor lithography?**

I think that from a technology decision point-of-view, the future of lithography is no longer in question. People know what they're going to do, from using double patterning to EUV lithography, for the next couple of technology generations.

Also, business leaders in the industry know that advanced lithography is going to happen. It requires a significant investment, but it's going to happen. And it's absolutely necessary for the semiconductor industry's health to continue advancing lithography technology, because it's what drives the growth of our industry.

Some people say it doesn't make a lot of sense to chase Moore's Law when it's getting so expensive to develop the equipment and capabilities to do so. Are we "tilting at windmills" here?

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The people who say that are not thinking about the big picture. They're not recognizing that we have a \$250 billion industry, and even though EUV may cost \$5 billion over five years or so, that's still half a percent of annual industry revenues.

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The reason for scaling is not because IDMs wanted to make transistors smaller; it's because scaling enabled them to make semiconductors more cost-effective. The economic corollary to Moore's Law is that the cost per transistor must go down. This continuing cost reduction acts as the real driver for Moore's Law. It's economic need that's driving technical innovation in the industry.

## **How important are alliances and consortia to achieving advanced lithography?**

They're absolutely critical. If you look back to when the cost to develop a successive technology was considerably lower, individual companies could afford to go it alone, with the rationale that it would provide them some kind of competitive advantage. As the overall cost of technology has increased and the number of companies that can afford it has steadily decreased, I think we've reached the point that even if companies can afford it, they realize that it's not in their best interest to pay for it themselves. If a given chip company is the only one that obtains a particular technology and it turns out there are competing technologies that can also be used,



they've paid for a single technology for no good reason. So it's much better if multiple partners can invest in the needed technology.

There's another really good reason. The number of lithography technologies has been reduced to a very small set. Essentially, there's only going to be one winner, and if that's the case, there's no way you can derive a competitive advantage. Once you come to that realization, it no longer makes sense to pay exclusively for a technology, or even pay the lion's share. It only makes sense to partner broadly and spend your energy convincing others to invest collectively instead of going it alone.

**What do you say to critics who assert that EUV will not be ready for volume manufacturing by 2013 and that the industry should go with double patterning, double exposure instead?**

Some manufacturers are using double patterning today, and if by doing so they can achieve products they can sell, then it makes economic sense for them. But for those chipmakers whose roadmaps rely upon being able to make denser pitch computer chips to maintain profitability, the only answer is for them to go with a technology that will allow them to meet their profitability goals.

The truth is that EUV is a single exposure lithography option for the next several technology nodes. For double patterning and its likely successors —multiple patterning, triple and quadruple patterning —the price structure is increasing geometrically with every technology node.

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**From a cost perspective, EUV has a tremendous advantage over double patterning and all its multiple patterning alternatives. That is the reason why EUV is, in fact, on the roadmaps of leading-edge semiconductor companies.**

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As to whether EUV will be ready in time, ASML [a Netherlands-based tool supplier] is on record as saying that they will have pre-production tools in 2010, and their first production tool is scheduled for delivery in 2012. Semiconductor companies are going to be using EUV to make chips and sell them as soon as these production tools are available. So yes, EUV is going to be on time.

**What's the current status of the EMI partnership?**

We started with six members, and we're currently at seven. Our efforts to include more players in the semiconductor manufacturing community are in full swing, and we're hoping to get additional members as time goes by. I'm very happy with the membership we have so far. Originally, I felt that we couldn't get started until we had at least five members, and we're significantly beyond that goal.

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**Our consortium has been making good progress toward enabling the infrastructure that it was created to address.**

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## Interview with Bryan Rice on SEMATECH Lithography continued

### **With EMI in place, are you confident that the industry will be able to develop mask inspection tools that will function below 22 nm?**

Yes, absolutely. I'm confident that the creation of this consortium will provide a mechanism for the industry to find answers to a continuing problem, which is small market size with high research cost infrastructure development. So EMI won't be limited just to mask inspection tools. I think we'll find that there will be other infrastructure elements that fall into the same category, and the existing stakeholders will already have a structure for fixing the next problem.

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**I think that a tool-funding consortium model is the right answer for many of the research and development problems that will be facing us in the future.**

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### **Could you give an example of those problems?**

One that comes to mind immediately is that mask write times are rapidly growing. It's generally accepted that if a write time goes past 24 or 48 hours, then it's simply not workable for a full-blown critical layer lithography mask. We're basically at that point with today's masks, and tomorrow's masks will exceed those write times. They may be pushing 72- to 96-hour write times.

So we really need a fast mask writer. From what I've seen, the only way to do that is with a multi e-beam advanced writer. That's an infrastructure development challenge that will

require an investment of multiple tens of millions of dollars; it's equivalent to the mask defect issues that EMI was created to address.

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**If we can get the broad support of the industry, we can add advanced mask writers to the EMI charter. So I think we've started something [at EMI] that's going to be around for a long time.**

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### **Summing up, what's the most important fact that people should know about SEMATECH's Lithography program?**

We're continuing to drive advancements in lithography technology. We're focused on EUV, and in particular we're concentrating on two goals: making sure that we have access to advanced imaging equipment so that resists and their associated materials continue to improve and are ready when our members need them, and secondly, providing the technical leadership in addressing the most difficult remaining challenge for EUV lithography, which is understanding and eliminating the sources of defects on EUV masks. We're focusing a tremendous amount of our energy making sure that the defectivity level is ready to support EUV lithography activities by the second half of this year.

# Industry Leaders at SEMATECH Litho Forum Expect EUV Lithography for Semiconductor Manufacturing in 2014

Lithography



At SEMATECH's Litho Forum, May 10-12, semiconductor business leaders and technology experts gained valuable insight on the industry's perceptions about and intentions for lithography development. The Forum, a three-day gathering of global lithography experts, featured an impressive line-up of senior executives and technical experts in the semiconductor industry who shared perspectives on why collaboration is imperative for semiconductor innovation and what challenges the development of next-generation technologies must tackle to make lithography successful.

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**“The fundamental enabler of the industry is improving the cost per function,” said Dan Armbrust, president and CEO of SEMATECH. “For the industry to evolve, business models need to take into account collaborations to control costs and extend current technologies while building the infrastructure for future solutions.”**

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Key highlights of the Forum included the following:

- Keynote speaker Gary Patton of IBM focused on the need for industry collaboration and innovation to continue the roadmap forward and pointed to SEMATECH's collaboration on EUV infrastructure as a good example of the type of collaborative innovation to make EUV happen.
- Presenters from IBM, TSMC, Tokyo Electron Limited, and GLOBALFOUNDRIES reviewed the current state of lithography and activities supporting lithography options, including EUV insertion, mask inspection challenges,

double patterning process development, multiple e-beam decisions for 22 nm and sub-22 nm, and overall tool readiness.

- Equipment and material suppliers emphasized that the overall development costs and risk reduction must be secured by ensuring that development progresses at a pace compatible with the EUV mask and resist infrastructure.

Additionally, more than 130 attendees were surveyed on their plans and preferences on lithographic approaches for future manufacturing. Key survey results included the following:

- As identified at previous Forums, 193 nm immersion double patterning continues to be the suitable lithographic technology for volume manufacturing in 2012.
- While some manufacturers will use the technology sooner, EUV would be capable of being placed into manufacturing in 2014, with extendibility into manufacturing in 2016.
- For immersion double patterning, cost of ownership, overlay capability, and extendibility to the next-generation device are still the top challenges.
- For EUV technology, mask defects, source power, exposure tool throughput, and cost of ownership were rated the top challenges.
- 193 nm and EUV were chosen as the technologies that would be considered for manufacturing at the 32 nm node or beyond.

With an industry cycle of about two years per lithography node, SEMATECH's biennial Litho Forum provides an opportunity for lithography users and suppliers to evaluate the progress of various technology options. The previous Forums helped coordinate industry consensus on the 32 nm half-pitch generation and beyond.

# SEMATECH Achieves Submicron 3D IC Bond Alignment Results in Integrated Bonding Tool Platform

*Key processes critical for building a strong infrastructure for volume production of TSVs*

Researchers from SEMATECH's 3D Interconnect program based at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex have reported advances in wafer-to-wafer bonding alignment accuracies through a series of tool and process hardening improvements. At the same time, the SEMATECH team has explored unique 3D metrology and failure analysis techniques to complement bonding tool development. These results are key steps towards bridging high-volume manufacturing readiness gaps for an integrated bonding tool platform and developing metrology techniques that will accelerate adoption of 3D integration technology. SEMATECH presented the results at the 2010 IEEE International Interconnect Technology Conference (IITC) on Wednesday, June 9, in Burlingame, CA.

Wafer-to-wafer (WtW) alignment and bonding are key enabling process steps for 3D interconnection of wafers through stacking. The International Technology Roadmap for Semiconductors (ITRS) roadmap for high density, intermediate level, through-silicon-vias with WtW bonding specifies via diameters of 0.8 to 1.5 $\mu$ m in 2012 and beyond. Post bond overlay accuracy of 0.5 to 1.0 $\mu$ m is necessary for these devices.

SEMATECH's 3D interconnect researchers have demonstrated submicron alignment accuracies for copper-to-copper (Cu-Cu) thermo-compression bonds and a variety of silicon-to-silicon and oxide-to-oxide fusion bonds without sacrificing bonding uniformity and bonding strength, using an integrated 300mm WtW pre-processing, aligning, and bonding tool. Additionally, to enhance process control, related metrology development on bonding interface defectivity and overlay metrology were reported. SEMATECH's latest achievements

are promising indications of the feasibility of meeting the WtW bonding roadmap as outlined in the ITRS.

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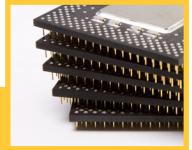
**“Through collaborative research, our goal is to develop and characterize new approaches to implementing 3D,” said Sitaram Arkalgud, director of SEMATECH’s 3D Interconnect Program. “These leading-edge results, which have a direct impact on processing costs, demonstrate SEMATECH’s leadership and innovative techniques that pave the way for low-cost 3D IC integration.”**

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With the rising demand for smaller, more functional and lower-power chips, 3D architecture is emerging as a leading solution for meeting leading-edge consumer device requirements. SEMATECH's 3D program was established at CNSE's Albany NanoTech Complex to deliver robust 300 mm equipment and process technology solutions for high-volume through-silicon via (TSV) manufacturing. To accelerate progress in realizing 3D's potential as a manufacturable and affordable technology for memory and CMOS manufacturers, the program's engineers have been working jointly with chipmakers, equipment and materials suppliers, and assembly and packaging service companies from around the world on early development challenges, including cost modeling, technology option narrowing, and technology development and benchmarking.

# SEMATECH Technologists Detail Process Advances to Accelerate 3D Manufacturing Readiness

## 3D Interconnect



With a focus on providing cost-effective and reliable solutions to speed manufacturing readiness of 3D technology options, experts from SEMATECH's 3D interconnect program based at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex outlined new developments in wafer bonding, copper removal, and wafer thinning at the 2010 Materials Research Society (MRS) Spring Meeting on April 5-9 in San Francisco, CA.

3D integration offers the promise of higher performance, higher density, higher functionality, smaller form factor, and potential cost reduction. In this emerging field, new and improved technologies and integration schemes will be necessary to realize 3D's potential as a manufacturable and affordable path to sustaining semiconductor productivity growth. At MRS, SEMATECH researchers described several practical 3D integration achievements – applicable across various 3D processes – in areas such as high-aspect ratio TSVs, wafer bonding, and thinning of interconnect test structures.

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**“Through collaborative research, our goal is to develop and characterize new approaches to implementing 3D,” said Sitaram Arkalgud, director of SEMATECH’s 3D Interconnect Program. “These practical approaches are critical to the integration, process development, metrology, and tool sets that will make 3D TSVs commercially viable.”**

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In partnership with the UAlbany NanoCollege, specific SEMATECH process advances aimed at improving 3D performance include:

- A practical approach to copper overburden removal by chemical mechanical polishing (CMP), using high removal rate slurry screening and achieving good planarization results, with low polish defects, at a rate suitable for emerging 3D TSV copper applications.
- The process development and associated metrology necessary in thinning bonded 300mm TSV and non-TSV bonded wafers, leaving a defect-free surface which meets the requirements for subsequent processing.
- An array of metrology techniques used in characterizing a manufacturable wafer bond process to deliver a void and dendrite-free bond for handle wafers.

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# ISMI ESH Experts Present Industry Data on Energy and Resource Conservation for Sustainable Manufacturing

In the effort to conserve energy resources and reduce costs of semiconductor manufacturing operations, ISMI Environment, Safety & Health (ESH) experts reported on energy efficient strategies, addressing both fab facilities and processing equipment for semiconductor manufacturing operations at the International High Technology Environment, Safety and Health Conference (IHTESH) on June 20- 24, 2010 in Hsinchu, Taiwan. The IHTESH is a multi-industry conference, attended by Semiconductor, PV, LED and TFT-LCD industries as well as government.

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**Researchers at ISMI's ESH Technology Center are focusing on new ways to recycle and reuse products both internally and externally while decreasing the amount of new materials needed for manufacturing. ISMI presentations at IHTESH outlined green building technologies and design, idle mode energy reduction methodology and process results, and approaches to development of key environmental performance indicators (KEPIs).**

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In an opening-day keynote speech ISMI's director, Joe Draina, outlined a historical perspective of ISMI initiatives and semiconductor ESH challenges ahead. Draina noted that in the next five years, some of the "same" ESH issues will continue, such as compliance with existing regulations,

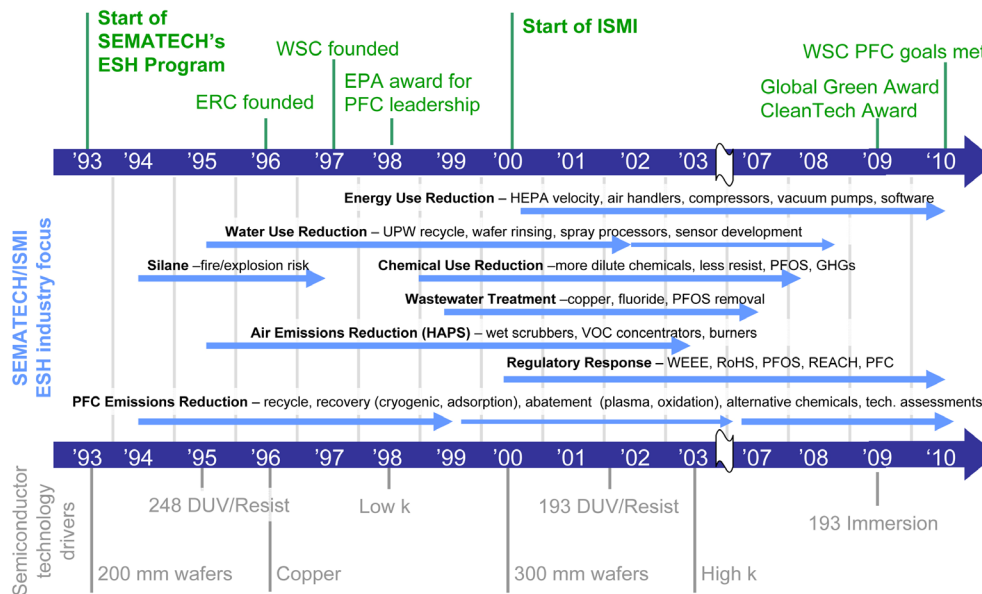
reduction of harmful fab emissions, and conservation of energy, water and chemical resources. Draina acknowledged that although semiconductor manufacturers have different needs, to effectively reduce ESH impacts manufacturers need to engage in cooperative projects to pursue a wide range of initiatives for sustainable manufacturing, industry environmental standards and green practices. In conclusion, Draina highlighted ISMI's ESH Center and its key role in continuing to lead and drive the industry's ESH efforts.

Additionally, in a series of three presentations, a team of ISMI ESH experts addressed the semiconductor-specific processes and energy reduction strategies, including:

- Benefits to implementation of potential credit towards LEED certification. LEED is a rating system developed by the United States Green Building Council (USGBC) that has emerged as the de facto approach to green building certification. Recognizing the critical importance of proactive environmental design for its members' fabs, ISMI reported on the development of fab-specific environmental performance criteria, including green building guidance for designers and operators of fabs.
- Process equipment energy reduction efforts have also focused on characterizing process equipment energy use during idle and processing modes, and demonstrating a low utility consumption idle mode for vacuum pumps and point-of-use abatement systems. The process equipment energy studies include the application of the SEMI S23 standard - A Guide for Conservation of Energy, Utilities and Materials Used by Semiconductor Manufacturing Equipment.



## ESH progress – ISMI historical



- One of the steps needed to advance energy reduction efforts was to develop a set of environmental performance indicators that quantify the key environmental impacts associated with the manufacture, use, and disposal of a product. ISMI reported a status on a set of KEPIs that quantitatively measures the environmental impact of semiconductor products. The KEPIs capture global warming, water use, chemical use, and waste generation impacts. When applied, they will provide the industry with a consistent set of product key environmental performance indicators.

For over a decade, the ESH Energy program at SEMATECH/ ISMI has characterized energy consumption in semiconductor facilities at both the fab and process level. To further dedicate itself to providing green technology solutions that lead to reduced energy consumption, ISMI formed the EHS Technology Center in 2009. The Center provides a broad-based, collaborative platform for developing better environmental practices for the industry, with goals of increasing efficiency and reducing costs in semiconductor operations.

# SEMATECH Makes Important Advances in Power and Performance Features for Next-Generation IC Devices

*SEMATECH technologists outline progress on innovative materials and processes for CMOS and emerging technologies*

SEMATECH engineers reported on materials and device structures that will define next generation CMOS and non-CMOS technologies at the 2010 Symposia on VLSI Technology and Circuits, June 15-18, at the Hilton Hawaiian Village in Honolulu, Hawaii.

Researchers at SEMATECH are focusing on techniques for simultaneously enhancing performance and reducing power consumption to enable the extension of CMOS logic and memory technologies. SEMATECH papers at VLSI, selected from hundreds of submissions, outlined new materials, processes and concepts, and described the way current semiconductor technologies can benefit from performance-enhancing features for future scaling needs.

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**“Identifying the optimum processes, materials, and device structures, and how they function when combined as a module, is of critical importance in pushing conventional CMOS scaling to its limits and paving the way for emerging beyond CMOS technologies,” said Raj Jammy, SEMATECH vice president of materials and emerging technologies. “The research that was presented at the VLSI symposium demonstrates SEMATECH’s leadership and innovative thinking as we help the industry develop future generations of low power, high performance IC devices that are both manufacturable and affordable.”**

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SEMATECH front-end process technologists reported the following technical advances:

- Investigating low contact resistance FinFETs with SOI substrates as a promising device structure for 22 nm and beyond: SEMATECH reported on a method to reduce parasitic resistance, a key issue affecting FinFET performance. While future narrow fin geometries reduce the area available for current flow through the silicon/silicide interface, reducing the interface barrier height in a simple and manufacturable way can realize significant performance improvements.
- Thoroughly exploring orientation and strain to enable a combination that simultaneously provides strong NMOS and PMOS: SEMATECH demonstrated a high mobility SiGe (110) channel CMOS with performance-boosting techniques. SEMATECH’s work advances high mobility channel CMOS technology with monolithic integration on a single SiGe (110)<110> channel orientation.
- Significant improvements in tunnel-FET transistors: In a project funded by DARPA and in collaboration with Prof. Chenming Hu of the University of California, Berkeley, SEMATECH researchers have enhanced this new class of devices aimed at lowering power dissipation in semiconductor devices. Tunneling transistors may be the answer to overcome the constraints posed by power dissipation in conventional CMOS scaling. SEMATECH reported an industry breakthrough—46mV/dec of sub-threshold swing—an important first step in realizing tunneling transistors.



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**In a short course series entitled, “Emerging Logic and Memory Technologies for VLSI Implementation,” Sitaram Arkalgud, director of SEMATECH’s 3D interconnect program, and Prashant Majhi, program manager of the CMOS scaling effort, presented on 3D interconnects and high mobility non-silicon channels.**

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Specifically, Arkalgud discussed process development, module integration, and the overall manufacturability outlook for via-mid through-silicon vias (TSVs), a front-end process that allows the interconnect length to be shortened as well as the bandwidth between the stacked chips to be increased, resulting in lower power, higher performance, and increased device density. Dr. Majhi described the critical need for high mobility non-Si channels to enhance performance and reduce the power dissipation in future CMOS devices. Furthermore, he outlined breakthrough results from SEMATECH’s FEP research team, which is leading a multi-pronged effort to demonstrate the feasibility of integrating high mobility III-V channel materials on a silicon platform and developing the infrastructure needed by the industry to implement such devices at future nodes.

In conjunction with VLSI, SEMATECH and IMEC co-hosted an invitational workshop entitled “High Mobility Channels” on June 17. In a series of presentations and panel discussions, the workshop featured experts from industry and academia debating the challenges and opportunities—from device, process, tooling, and metrology perspectives—related to large-scale III-V manufacturing on silicon in a CMOS

environment. Majhi shared highlights of SEMATECH’s efforts and its success in developing a fully functional test vehicle in a 200 mm flow. Several other industry experts and leading faculty researchers presented the results of their work. The panel of experts and audience concluded that III-V on Si is a next step in the evolution of Si CMOS and perhaps is necessary to keep power down in future generation chips.

The Symposium on VLSI Technology and Circuits is one of many industry forums SEMATECH uses to collaborate with scientists and engineers from corporations, universities, and other research institutions that are key to SEMATECH’s ambitious research endeavors. It is sponsored by the IEEE Electron Devices Society and Solid-State Circuits Society and the Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers.

# ISMI Workshop Provides ‘Real Life’ Implant Equipment Solutions for Next Generation Device Manufacturing

*Industry participants receive feedback on productivity challenges and system techniques*

Device manufacturers gathered to explore ‘real life’ ion implantation equipment solutions for next generation device manufacturing at ISMI’s Implant Equipment Workshop on April 20-21 in Boston, MA. The workshop is a part of the 2010 ISMI Installed-base Equipment Series.

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**In this workshop, ISMI brought together integrated circuit (IC) manufacturers, original equipment manufacturers (OEMs), alternate source providers, and experts on implant source gases, metrology and beam design to discuss key productivity and cost issues associated with ion implant equipment. Through sharing real fab experiences, including best-known-methods, participants determined critical equipment issues, and benchmarked equipment performance metrics on maintenance, equipment engineering, and parts challenges.**

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“The productivity of an implanter is important to the bottom line, and innovative implant technologies, in particular, are crucial for meeting the needs for finer fabrication, higher integration densities, and faster speeds in next-generation semiconductor devices,” said Tres Greenwade, ISMI project manager and workshop chair. “Our workshop attendees received real-time feedback on top equipment issues and benchmark equipment performance metrics, and went back

to their companies with tangible solutions to several specific installed-base implant equipment challenges.”

Highlights from ISMI’s Implant Equipment Workshop include the following:

- Data-driven sessions which provided feedback on equipment performance
- Ranked critical issues which were shared between device manufacturers and relevant OEMs
- Updates on critical equipment productivity challenges for current and next generation processes, and on design challenges of next generation equipment
- Participant reports on “Golden Nuggets” of productivity and cost-cutting methods that can be readily applied in fabs of various wafer sizes, on topics ranging from implanter dedication and implant source cross contamination to new arc chambers.

The cost of new semiconductor fab equipment and the challenges of device leakage, shallow junction creation, and device shrinkage are pushing the limits of Moore’s Law. ISMI will host a series of Installed-base Equipment workshops throughout 2010, each focused on improving productivity and reducing costs in a particular tool type. The Implant Equipment Workshop is the second in this series; the Thermal Equipment Workshop, which took place in Austin, TX on March 23-25, reviewed top thermal issues in Furnace and RTP equipment.



# ISMI MANUFACTURING WEEK 2010

The only conference focused on productivity and cost-savings solutions that can be implemented immediately in today's fabs.

## **AEC/APC Symposium**

November 1 - 3, 2010 | Austin, TX

## **ISMI Symposium on Manufacturing Effectiveness**

November 3 - 4, 2010 | Austin, TX

[www.ismi.semtech.org/ismisymposium](http://www.ismi.semtech.org/ismisymposium)

# SEMATECH Knowledge Series 2010

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Semiconductor technologists from a wide range of fields can join the search for solutions to the industry's most challenging issues at the 2010 SEMATECH Knowledge Series (SKS) of meetings, workshops, and symposia.

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SKS meetings are highly interactive and allow attendees to:

- Review and rank critical issues in bringing R&D concepts to high volume manufacturing
- Focus on ways to extend the use of incumbent materials and technologies
- Share data and methodologies for lowering costs and improving productivity in current and next-generation fabs through advances in equipment, processes, resources, design, and manufacturing methods
- Guide the industry in seeking effective solutions for future technology generations
- Build on critical university, supplier, and manufacturer relationships needed for accelerated innovation

All SKS meetings are open to the public, with several accepting sponsorships and exhibits. Additional meetings may be added during the year.

## Lithography

### **SEMATECH Advanced Mask Cleaning Workshop**

This full-day workshop provides a forum for SEMATECH members, mask and wafer cleaning suppliers, and researchers to discuss advancements in technologies and solutions applicable to advanced mask cleaning and surface preparation challenges. Topics include sub-30nm particle removal, molecular contamination removal, mask inspection defect analysis, and environmental approaches to mask cleaning. Held in conjunction with the SPIE/BACUS Symposium.

13 September 2010; Monterey, California

### **2010 International Symposium on Extreme Ultraviolet Lithography**

The EUVL Symposium is part of SEMATECH's ongoing commitment to help mature the technology and infrastructure for extreme ultraviolet lithography (EUVL), including sources, masks, optics, resists, contamination control, and metrology to support EUVL pilot line manufacturing requirements. The symposium is hosted by Selete, EUVA, SEMATECH and IMEC.

17–20 October 2010; Kobe, Japan

### **SEMATECH Workshop On Directed Self-Assembly**

This full-day workshop, which will be held in conjunction with the 2010 International Symposium on Lithography Extensions, will include a series of presentations by experts in device design, lithography, and semiconductor processing on the potential application of directed self-assembly to semiconductor manufacturing as a candidate to extend optical lithography. DSA technology combines lithographically defined features to guide self-assembled polymers by physical or chemical properties to create features smaller than those possible with optical lithography.

20 October 2010; Kobe, Japan

### **2010 International Symposium on Lithography Extensions**

The Lithography Extensions Symposium focuses on efforts to extend 193nm lithography to the 22nm half-pitch node and beyond. The primary emphasis will be on patterning processes that enable pitch division, techniques for improving process control, and emerging technologies that will extend optical lithography. SEMATECH in collaboration with IMEC and Selete will host the symposium, which will be held with the EUVL Symposium.

21–22 October 2010; Kobe, Japan

### **Advanced Technologies**

#### **SEMATECH Workshop on Stress Management for 3D ICs Using Through Silicon Vias**

Copper-filled TSVs and wafers thinned to a few tens of microns modify the stress profiles in the silicon and exacerbate the stresses introduced by tier-to-tier bonding and chip-package interactions. This workshop will bring together representatives from device manufacturers, electronic design automation suppliers, semiconductor assembly and test service providers, and the R&D community to develop a unified vision of a simulation based DFM flow for mechanical stress management for advanced TSV-based 3D products and to reach consensus on a uniform design kit format and content.

13 July 2010; San Francisco, California

#### **SEMATECH Workshop on Metrology for 3D Interconnect**

Successful introduction of 3D interconnects will require that equipment suppliers and device manufacturers overcome the inherent challenges associated with measuring opaque films and high-aspect ratio features that dominate 3D architectures.

Metrology for 3D architectures requires new techniques, revisiting and improving some older techniques, and breakthrough innovations to create new metrology tools. This workshop, held in conjunction with SEMICON West, focuses on how new and existing wafer metrology technologies can be utilized, modified, or enhanced to measure and improve 3D interconnect processes..

14 July 2010; San Francisco, California

#### **SEMATECH International Symposium on Advanced Gate Stack Technology**

The focus of this year's annual symposium is "Functional Stacks for Logic and Memory Devices." The exploration of functional stacks for future (sub 22nm node) devices will include high-k/metal gate stacks for Si, SiGe, III-V high performance MOSFETs; metal/high-k/metal gate stacks for storage capacitors and resistive change memory; high-k/metal gate for flash memory; insulators and metals needed for high-performance NEMS and sensors; and magnetic material stacks needed for spin-based devices. The symposium will feature industry experts presenting their latest research in both invited and contributed talks and a discussion panel of representatives from major semiconductor device makers, equipment makers, and academia.

29 September - 1 October, 2010; Albany, New York

### **Manufacturing**

#### **ISMI Manufacturing Weeks**

This year's ISMI Manufacturing Week in Austin now includes the ISMI AEC/APC Symposium, followed by the 7th Annual ISMI Symposium on Manufacturing Effectiveness, as well as an extensive variety of workshops and short courses focused on specific topics relevant to today's semiconductor

## SEMATECH Knowledge Series 2010 continued

manufacturing challenges. Additional information about the latest products, services, and novel ideas for increasing profits can be found at the supplier exhibits throughout the week. Similar ISMI Manufacturing Week events will take place in Taiwan and Japan, in conjunction with the SEMATECH Symposia to be held this fall.

ISMI Manufacturing Week North America – 31  
October-4 November 2010; Austin, Texas

ISMI Manufacturing Week Taiwan – 6-10  
September 2010; Hsinchu, Taiwan

ISMI Manufacturing Week Japan – 13-  
15 September 2010; Tokyo, Japan

### **ISMI Symposium on Manufacturing Effectiveness**

The ISMI Symposium on Manufacturing Effectiveness is the semiconductor industry's most important event for exchanging ideas about real-time, cost-saving solutions to help improve manufacturing productivity. The 7th Annual Symposium will be held during ISMI Manufacturing Week.

3-4 November 2010; Austin, Texas

### **ISMI AEC/APC Symposia**

These symposia, focused on advanced equipment control and advanced process control (AEC/APC), bring IC manufacturers and suppliers together to accelerate the industry toward more efficient and more intelligent manufacturing through automated data-driven decision making.

ISMI AEC/APC Symposium North America (held during ISMI Manufacturing Week, see above) – 31  
October-3 November 2010; Austin, Texas

Joint Symposium of e-Manufacturing & Design Collaboration 2010 and AEC/APC-Asia 2010 (a partnership between TSIA and ISMI) – 2-3 September; HsinChu, Taiwan

### **ISMI Installed-base Equipment Series - 2010**

The 2010 ISMI Installed-base Equipment Series is an equipment productivity forum for integrated circuit (IC) manufacturers and original equipment manufacturers (OEMs) to discuss key productivity and cost issues in a series of workshops focused on specific wafer fabrication equipment types. In addition, selected experts will be invited to present their unique perspectives on topics related to the various tool types.

CVD Equipment Workshop - 22-24 June  
2010; San Jose, California

Etch Equipment Workshop - 13-15 July  
2010; San Francisco, California

Photo Equipment Workshop - 13-14  
September 2010; Tokyo, Japan

Wet Processing Equipment Workshop - 28-  
30 September 2010; Austin, Texas

Metrology Equipment Workshop - 5-7  
October 2010; San Jose, California

PVD Equipment Workshop - 12-14  
October 2010; San Jose, California

CMP Equipment Workshop - 16-18  
November 2010; San Jose, California

### **ISMI Next Generation Factory e-Manufacturing Workshops**

Organized by ISMI with support from SEMI, these workshops will provide the vision, progress, and roadmap for next generation factories, as well as reports on enabling implementations and deployment experiences, including the latest Interface A, equipment data quality/time synchronization, predictive maintenance, and Enhanced Equipment Quality Assurance (EEQA) requirements. These workshops provide an excellent opportunity to further align IC manufacturers and suppliers in their next generation factory and e-manufacturing implementation strategies as the semiconductor industry strives to continuously improve factory productivity.

Summer Workshop (held in conjunction with SEMICON West) – 14 July 2010;  
San Francisco, California

Winter Workshop (held in conjunction with SEMICON Japan) – 30 November 2010; Makuhari Messe, Chiba, Japan

### **Other Industry-wide Events**

#### **SEMATECH Symposia - 2010**

Senior executives and managers from SEMATECH and ISMI will hold symposia in Taiwan and Japan, in conjunction with ISMI Manufacturing Week events, to present program updates and examples of how SEMATECH's models for consortial R&D are accelerating the next technology revolution worldwide. Public sessions will focus on key technology, manufacturing, and business issues in today's global semiconductor industry,

with opportunities for networking; member-only sessions will be devoted to reviewing program activities, technology transfer, and member feedback.

SEMATECH Symposium Taiwan 2010 – 7  
September 2010; Hsinchu, Taiwan

SEMATECH Symposium Japan 2010 – 15  
September 2010; Tokyo, Japan

#### **International Technology Roadmap for Semiconductors (ITRS) Conferences**

The ITRS will be reviewed in 2010 for updates to the technology requirements tables and other key data. The ITRS public conferences offer technologists and strategists from the manufacturing and supplier communities the opportunity to participate in building the next ITRS by providing input to the working group teams of industry and research experts who revise the semiconductor industry roadmap.

Summer Conference (held in conjunction with SEMICON West) – 14 July 2010; San Francisco, California

Winter Conference (held in conjunction with SEMICON Japan) – 3 December 2010; Makuhari Messe, Makuhari, Japan

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