



# TECH *report*

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*Accelerating the next technology revolution*

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# Realizing the 450 mm Transition



**Dan Armbrust,**  
**SEMATECH**  
**President and CEO**

The recent announcement of the new 450mm consortium (Global 450mm Consortium or G450C) is excellent news for our industry, for the region, and for SEMATECH, as 450mm development takes a huge step forward.

The investment marks a very important milestone for the semiconductor industry. It will play a vital role in accelerating the industry's transition to the next wafer size, and will build on and expand our strong government-industry-university alliance with New York State and CNSE.

As we take in the significance of this new initiative, we certainly want to recognize our member companies for their investment in ISMI's successful 450mm program, which has helped build the foundation for the new consortium. Our program has played a critical role in coordinating industry efforts on wafer supply, standards setting, test wafer generation and equipment demonstration. With the support of our members, many of the capabilities required to enable the 450mm transition are now in development, and industry momentum is accelerating rapidly in all areas of the supply chain.

We also recognize New York State's vision and continued commitment to investing in the future and serving as a catalyst for 450mm development. The new initiative will be based here in New York, and the College of Nanoscale Science & Engineering (CNSE) at the University at Albany SUNY will provide state-of-the-art facilities that member companies will use for wafer testing, tool demonstrations and process technology development to enable a cost-effective 450mm transition.

This announcement will result in significantly increased participation of the industry supply chain, with new possibilities to develop innovative collaborations. SEMATECH has been the collaborative leader in driving the evolution of our industry, and the 450mm transition represents another once-in-a-generation opportunity. Further, as the transition to the next wafer size is realized, our vision is that SEMATECH will be a key partner in the use of the 450mm capabilities to perform advanced technology R&D and manufacturing improvements with a greater diversity of partners and members.

We look forward to extending our partnership with New York State, CNSE and the other G450C members by building on the continued successes of our 450mm program, and accelerating this important technology revolution.

Daniel Armbrust  
President and CEO, SEMATECH

# SEMATECH Showcases Advanced and Emerging Semiconductor and Manufacturing Technologies in East Asia

SEMATECH and ISMI held its 7th annual Japan Symposium and regional meetings on June 22-24 and its 4th annual Taiwan Symposium and related sessions on September 13-15. Together, the symposia hosted approximately 800 members of the Japanese and Taiwanese semiconductor community, including device manufacturers, equipment and materials suppliers, and university researchers.

Focusing on critical areas of advanced and emerging technologies, these events featured an impressive lineup of almost 100 presentations given by senior executives and technical experts from SEMATECH and the semiconductor industry who shared perspectives on current and future business trends/challenges in semiconductor R&D and manufacturing. Attendees were offered a series of in-depth technical sessions highlighting progress on key industry issues in the areas of 3D, EUV, advanced devices, emerging technologies, metrology, 450mm and manufacturing productivity.

“Global collaboration is the key to our industry’s long-term success, especially given the current economic challenges, and we look forward to continuing the many excellent relationships we have forged with

members, partners and colleagues in Asia,” said Dan Armbrust, SEMATECH president and CEO. “The SEMATECH Symposia are forums for exchanging ideas on how we can work together to speed the development of advanced technology and improve manufacturing productivity while lowering costs.”

To complete the East Asia Symposia tour, SEMATECH and ISMI hosted the 2nd annual Korea Symposium in Seoul on October 27-28 in cooperation with Korea’s National Semiconductor Day events. The two-day public event, organized by COSAR and attended by over 300 participants from the Korean semiconductor community, included an additional 20 presentations highlighting achievements in advanced and emerging technologies and new opportunities for global collaboration.

Keynote speakers were Sung-Ki Park, Director, Hynix Semiconductor; Choon-Heung Lee, Corporate Vice-President, Amkor Technology; and Dan Armbrust, President and CEO, SEMATECH.

During the course of the event, SEMATECH and ISMI offered a series of six technical sessions which outlined progress and challenges in the areas of EUV lithography, 3D interconnects, advanced devices, 450mm and manufacturing productivity.



# SEMATECH Makes a “Triple Play” with October’s SEMATECH Knowledge Series (SKS) Conferences

While October is widely acclaimed in the U.S. for major league baseball’s crowning event—the World Series—it was also shaping up to be a very prodigious month for the SEMATECH Knowledge Series (SKS) with three major industry conferences hosted either in full or in part by SEMATECH and ISMI, all taking place during the week of October 17-21.

The 2011 International Symposia on Extreme Ultraviolet Lithography and Lithography Extensions, ISMI’s Manufacturing Week, and the International Symposium on Advanced Gate Stack Technology are three of the biggest events in the SEMATECH Knowledge Series, a suite of forums designed to explore the industry’s critical issues, build industry consensus and drive actionable solutions.

## International Symposium on Extreme Ultraviolet Lithography and the International Symposium on Lithography Extensions

For the second consecutive year, the International Symposium on Extreme Ultraviolet Lithography and the International Symposium on Lithography Extensions were strategically co-located in order to bring together the industry’s top experts and researchers to address the challenges

associated with the development and implementation of these critical lithography technologies. The joint symposia took place in Miami, Florida beginning with the EUVL Symposium on October 17-19, followed by the Symposium on Lithography Extensions on October 20-21. Related technical working group meetings were also scheduled during the week.

### Keynote and invited speakers at the EUVL Symposium included:

- John Y. Chen, NVIDIA Corporation (plenary speaker) - “Transform Designs to Chips with Sub-20nm Technologies”
- Han-Ku Cho, Samsung (keynote) - “EUV Readiness and ASML NXE3100 Performance”
- Emily Gallagher, IBM - “EUV Masks: Ready or Not?”
- Eric Hendrickx, IMEC - “From ASML Alpha Demo Tool to ASML NXE:3100 at IMEC, EUV Lithography Heading Towards Pre-Production”
- Masamitsu Itoh, Toshiba - “Critical Assessment of Mask Readiness”
- Ted Liang, Intel - “Critical Assessment of Substrate and Mask Blank Readiness”



- Greg Wallraff, IBM - “Fundamental Resist Limits”
- Tony Yen, TSMC - “ASML NXE3100 Performance”

The keynote at the Lithography Extensions Symposium was delivered by Risto Puhakka of VLSI, who spoke on “The Business of Commercializing Innovation.”

### ISMI Manufacturing Week

The ISMI Manufacturing Week featuring the 8th annual ISMI Symposium on Manufacturing Effectiveness, took place during the week of October 17-21 in Austin, Texas. The week kicked off with a series of short courses and workshops followed by the ISMI Symposium which featured two full days of technical sessions focusing on strategies and solutions for increasing productivity and reducing manufacturing expenses.



*ISMI Manufacturing Week*

Symposium topics included: advanced process control, green manufacturing, emerging ESH regulations, factory productivity, yield and metrology, overall equipment effectiveness, factory simulation, nanomaterials bio-safety, and statistical methods.

#### **Keynote speakers at the ISMI Symposium included:**

- Paul Fego, Texas Instruments - "Building Blocks for an Efficient and Effective Manufacturing Model"
- John Scoville, Applied Materials - "Predictability as a Key Component of Productivity: The Move Towards Smart Yield"

Manufacturing Week also featured three days of exhibits by some of the industry's premier software, equipment, and spare

parts companies exhibiting their unique solutions for increased fab productivity.

#### **8th International Symposium on Advanced Gate Stack Technology**

SEMATECH's 8th International Symposium on Advanced Gate Stack Technology, which took place October 19-21 in Bolton Landing, New York, focused on functional stacks for future (sub-15 nm node) logic and memory devices, including high-k/metal gate stacks for Si, Ge, III-V high-performance MOSFETs; metal/high-k/metal gate stacks for high-k/metal gate for flash memory metals; and magnetic material needed for spin-based devices.

The symposium featured over 30 invited talks from industry experts who presented recent developments in:

- Gate stacks on non-silicon
- Interface traps and defects on non-silicon
- RRAM
- STT-MRAM and magnetic logic
- Non-planar silicon
- Tunnel FET

#### **Keynote speakers during the three-day event included:**

- Jungdal Choi, Vice President, Flash Memory, Samsung
- Kelin Kuhn, Intel Fellow
- Scott Thompson, Professor, University of Florida



## SEMATECH Appoints GLOBALFOUNDRIES Veteran Stefan Wurm Director of Lithography

In September, SEMATECH appointed GLOBALFOUNDRIES assignee Dr. Stefan Wurm as director of Lithography, succeeding Bryan Rice, who recently accepted a position as SEMATECH's director of Strategic Initiatives. The announcement of Wurm's appointment however, did not surprise industry insiders, many of whom have long known Wurm for his firm commitment to the development of extreme ultraviolet lithography (EUVL) as a feasible alternative technology for next-generation lithography.

Wurm, an industry veteran with over 20 years of experience in the industry, has had a long and distinguished career with SEMATECH. He initially joined the consortium as an assignee from Siemens in 1997 working on 300 mm metrology tool equipment demonstrations for the International 300 mm Initiative (I300). After the completion of his first assignment at SEMATECH, Wurm returned briefly to Infineon (formerly Siemens) in Munich, Germany before initially becoming involved in EUVL technology as the Infineon assignee at the Extreme Ultraviolet Lithography Limited Liability Company (EUV LLC) in Livermore, CA.

In September 2003, his passion for EUVL technology brought Wurm back to

SEMATECH where he initially served as senior EUVL technologist before taking on the position of EUV Strategy Program manager in 2004. In this role, Wurm was instrumental in shaping and directing the EUVL program with the ultimate goal of providing industry-wide infrastructure capabilities necessary for high-volume manufacturing, including EUV source technology and metrology for source evaluation; mask blank development and mask infrastructure readiness; EUV resist materials and processes that meet stringent resolution, linewidth roughness and sensitivity specifications; and the development of metrology tools needed for detecting defects in advanced EUVL masks.

Wurm was promoted in 2008 to associate director of SEMATECH's Lithography division, where he worked alongside Bryan Rice to continue building the EUV program and focus on the development of other alternative lithography solutions such as nanoimprint.

As SEMATECH's newest lithography director, Wurm is committed to continuing the effort to ensure that SEMATECH's strategic direction and its execution support the critical lithography technologies required to enable continued scaling.

**Q. It's well known that you have been a long-time EUVL advocate, dedicating nearly one-third of your career in the semiconductor industry to the development of extreme ultraviolet lithography. Why are you so passionate about this particular technology?**

**A.** When I made the decision to start in EUV it was the most exciting technical field I could see, as this technology was still very much in the fundamental research stages and I was intrigued by the challenge of how we would make this become a reality. There are few opportunities where one has the chance to contribute to the success of such a game-changing technology as EUV.

**Q. For many years now, you've played an active role in SEMATECH's partnership with other industry organizations such as Imec and EIDEC in hosting the annual International Symposium on Extreme Ultraviolet Lithography, which is now in its 10th year. In your opinion, how has this event evolved over the years and what role has this type of global industry approach played in the advancement of EUVL technology?**

**A.** Developing a complex technology like EUV is truly an international effort with many players involved. It has been fascinating to see how research institutions,

consortia and companies have worked together in this way. Over the years, the EUVL Symposium has served as an industry-wide clearinghouse for a broad range of ideas, where participants identify and rank the critical issues in order to more effectively determine where to focus research efforts. It has really helped to foster collaboration among the various industry stakeholders and build the consensus needed to further EUV progress.

**Q. The development of EUVL has been a slow and arduous process, commanding considerable time and effort to get the technology to the point where it is now. What do you see as the final impediments that must be overcome in order to successfully insert EUVL into high-volume manufacturing?**

**A.** First of all, we have to increase productivity to a level that it will meet manufacturing requirements. That means increasing EUV source power by ~ 20X over the next 1-2 years. Once that is achieved, the industry must have yielding masks with no or very few defects. In the longer run, we need to continue the development of new resist materials to be able to transfer the aerial image generated by EUV scanners into ever smaller patterns on the wafer.

**Q. Your career in the semiconductor industry has spanned nearly a quarter of a century and you've seen many different manufacturing technologies come and go. In the future, what direction do you think the industry will take in order to successfully achieve "More than Moore"?**

**A.** Looking back to when I first started, the industry has become far more diverse with respect to markets and products. With each device generation, we not only continue to adapt, but deliver even more functionality (just think about today's cell phone—nobody knew about that 20 years ago, right?). It really is not clear where this will end, as designers continue to come up with device designs that they believe will work at feature sizes as small as 5 nm. So consequently, we have to continue to develop manufacturing and lithography solutions that can produce those devices. For the next 10-15 years, though, I still see lithography as the critical enabler of the continued effort to shrink feature sizes, although other technologies such as 3D-integration and systems integration on single chips will also enable very aggressive scaling. So, it is really a combination of "Moore" and "More than Moore" that will continue to change our lives in many ways yet to be known.

### Bryan Rice Appointed Director of Strategic Initiatives



Bryan Rice has been appointed SEMATECH's director of strategic initiatives. In his new role he will be responsible for identifying effective strategies that will extend SEMATECH's core missions through the next 5-7 years.

Rice, who most recently served as director of Lithography, has been on assignment to SEMATECH from Intel Corporation since 2006.

Under his new leadership, Rice will examine and identify ways to extend SEMATECH's capabilities, and to effectively align the company's business goals with existing member and industry needs. This applies to SEMATECH's four core programs—Front End Processes, Lithography, Metrology, and 3D Interconnect—as well as possibly creating new programs that exploit synergies between those existing divisions.

# SEMATECH to Showcase Innovations in Gate Stacks, FinFETS and Resistive RAMS at IEDM 2011

Technical papers to demonstrate emerging solutions for critical material and device technologies

Engineers from SEMATECH's Front End Processes (FEP) program are scheduled to present four technical papers and participate in a panel discussion at the 57th annual IEEE International Electron Devices Meeting (IEDM) from December 5-7, 2011, at the Hilton in Washington, D.C.

Highlighting significant breakthroughs that address the growing need for higher performance and low-power devices, SEMATECH experts will report on resistive RAM (RRAM) memory technologies, high-mobility channel materials, and advanced Fin for scaled CMOS devices on 300mm silicon wafers.

## SEMATECH Presentations:

### *Comprehensive Physical Modeling of Forming and Switching Operations in HfO<sub>2</sub> RRAM Devices*

**When:** Tuesday, December 6, 4:00 p.m.

**Where:** Jefferson Room

This paper will examine a novel physical model of RRAM devices that allows describing the creation of the CF during forming and the electrical transport in HRS and LRS within the same unified approach.

### *Improved High-k/Metal Gate Lifetime Via Improved SILC Understanding and Mitigation*

**When:** Tuesday, December 6, 3:10 p.m.

**Where:** Lincoln Room

This paper will identify, for the first time, key factors impacting SILC through a comprehensive reliability study for high-k/metal gate nMOSFET with several mitigating process changes. A direction to SILC reduction, thereby improving device lifetime, will be proposed.

### *ALD Beryllium Oxide: Novel Barrier Layer for High Performance Gate Stacks on Si and High Mobility Substrates*

**When:** Wednesday, December 7, 9:30 a.m.

**Where:** Columbia 5 and 7

This paper will show an analysis of the BeO films epitaxially grown on the Si and GaAs substrates using a conventional ALD technique. The superior physical and electrical properties of the BeO films demonstrate the feasibility of employing this novel oxide as a gate dielectric and barrier layer in the gate stacks in the manufacturing environment.

### *300mm FinFET Results Utilizing Conformal, Damage Free, Ultra Shallow Junction (X<sub>j</sub>~5nm) Formed with Molecular Monolayer Doping Technique*

**When:** Wednesday, December 7, 3:15 p.m.

**Where:** Columbia 5 and 7

This paper will demonstrate a of a new, conformal, damage free doping technique (monolayer doping) of a 20nm FinFET. This technique is very promising to address key

FinFET scaling issues: series resistance and short channel control for 15nm node and beyond.

## Panel Session:

### *Is Three Dimensional Integration at Best a Niche Play?*

**When:** Tuesday, December 6, 8:00 p.m.

**Location:** International Ballroom Center

Sitaram Arkalgud, SEMATECH's director of Interconnect, will join other distinguished industry experts, including Shekhar Borkar of Intel, SiYoung Choi of Samsung, John Lau of ITRI, and Jan Vardaman of Techsearch, Inc. The panel, moderated by Subramanian Iyer an IBM Fellow, will explore critical 3D issues from each panelist's perspective, and evolve into an open discussion with audience participation.

The IEDM conference draws an international audience of industry professionals for an intensive exploration of design, manufacturing, physics, and modeling of semiconductors and other electronic devices. The conference spotlights leading work from the world's top electronics scientists and engineers; it is one of many industry forums SEMATECH uses to collaborate with scientists and engineers from corporations, universities, and other research institutions, many of whom are research partners.

# SEMATECH Orchestrates 3D Interconnect Standards Activities

Online information sharing solution enables 3D IC industry to define and track the development of high-volume manufacturing standards

SEMATECH has announced a new online 3D Standards Dashboard solution to help meet the demand for an open, centralized forum for members of the 3D interconnect community to discuss and exchange information on standards activities. The 3D Standards Dashboard aims to promote the development of standards and encourage widespread participation in standardization efforts for heterogeneous 3D integration. Standards development organizations (SDOs) participating in the 3D Dashboard include IEEE, JEDEC, SEMI, and Si2.

Due to the tremendous benefits of higher performance, increased functionality, and cost reduction, adoption of 3D integration is rapidly spreading to a wide variety of companies across the semiconductor and MEMS industries. Despite its high potential, a lack of uniform standards and a limited understanding of key manufacturing parameters threaten to delay introduction of high volume products such as wide I/O DRAM for mobile applications.

The set of standards required by the industry are broad in scope and standardization activities span many different groups, resulting in a very large and complex standards landscape. The challenge for the standardization community is to improve information sharing of standardization

processes to accelerate the development and adoption of 3D standards.

The 3D Standards Dashboard, initiated and managed by SEMATECH's 3D Enablement Center, provides a definitive resource that enables information sharing and communication of 3D standard activities across the supply chain. Companies involved in 3D production can use the 3D Standards Dashboard to find existing standards as well as to identify and track standards development activities in areas such as design, testing and production. Additionally, the 3D Standards Dashboard provides a proactive forum for facilitating collaborative discussions on perceived gaps in standardization activities and for identifying which SDO will best meet the need for a specific standardization activity.

"The development and adoption of 3D standards to ensure interoperability will require collaboration and participation across the supply chain, particularly more communication and information sharing between the design, test, and manufacturing communities," said Larry Smith, Enablement Center manager. "The main objective of the 3D Standard Dashboard is to have a public and centralized

forum for SDOs involved in standards development to identify risk areas and determine gaps related to all necessary standards for 3D interconnects."

In 2010, SEMATECH teamed with the SIA and SRC to establish the 3D Enablement Center—a first-of-its-kind effort to drive industry standardization efforts and technical specifications for heterogeneous 3D integration. The Enablement Center plays a strategic role by providing the necessary infrastructure for the entire industry to leverage 3D packaging technology for innovative new applications.

The 3D Standards Dashboard can be accessed at:

<http://wiki.sematech.org/3D-Standards>



# Governor Cuomo Announces \$4.4 Billion Investment by International Technology Group to Develop Next Generation Computer Chip Technology in New York

Thousands of jobs will be created or retained in Albany, Canandaigua, Utica, East Fishkill, and Yorktown Heights; New York State wins investment over countries in Europe, Asia and the Middle East

Governor Andrew M. Cuomo recently announced that New York State has entered into agreements providing for investments valued at a total of \$4.4 billion over the next five years from five leading international companies to create the next generation of computer chip technology.

The five companies involved are Intel, IBM, GLOBALFOUNDRIES, TSMC and Samsung. New York State secured the investments in competition with countries in Europe, Asia and the Middle East.

The agreements mark an historic level of private investment in the nanotechnology sector in New York. Research and development facilities will be located in Albany, Canandaigua, Utica, East Fishkill and Yorktown Heights. In addition, Intel separately agreed to establish its 450mm East

Coast Headquarters to support the overall project management in Albany.

“This unprecedented private investment in New York’s economy will create thousands of jobs and make the state the epicenter for the next generation of computer chip technology,” Governor Cuomo said. “IBM, which is celebrating 100 years in New York, Intel, which is making its most significant investment in New York, as well as TSMC, GLOBALFOUNDRIES and Samsung now recognize that the state is on its way to becoming a premier location for jobs, which is why these companies are making this major investment. In the last nine months, my administration has worked to create a more confident environment for doing business in New York, and major deals like this one prove that the state is truly open for business.”

The investment in these two efforts will result in the creation and retention of approximately 6,900 jobs. That number includes 2,500 additional high-technology positions comprising of:

- 800 at CNSE Albany NanoTech Complex
- 950 at IBM - Yorktown Heights and IBM - East Fishkill



- 450 at SUNY Institute of Technology (SUNYIT) in Utica
- 300 at CNSE's Smart System Technology & Commercialization Center in Canandaigua

In addition, approximately 1,500 construction jobs will be created in Albany and 400 in Utica. As a result of the investment 2,500 existing jobs in Albany, Canandaigua and East Fishkill will be retained.

No private company will receive any state funds as part of the agreement. To support the project, New York State will invest \$400 million in the SUNY College for Nanoscale and Science Engineering (CNSE) in Albany, including \$100 million for energy efficiency and low cost energy allowances. The state investment in CNSE will be made over a five-year period. The state investment will be directed entirely to CNSE, and all

tools and equipment acquired through the investment will be owned by CSNE.

The investment in the state is made up of two projects. The first project, which will be led by IBM and its partners, will focus on making the next two generations of computer chips. These new chips will power advanced systems of all sizes, including, among other things, computers and national security applications. This new commitment by IBM brings its total investment in chip technology in New York to more than \$10 billion in the last decade.

The second project, which is a joint effort by Intel, IBM, TSMC, GLOBALFOUNDRIES and Samsung, will focus on transforming existing 300mm technology into the new 450mm technology. The new technology will produce more than twice the number of chips processed on today's 300 mm

wafers thus lowering costs to deliver future generations of technology with greater value and lower environmental impact.

This investment will have other beneficial economic impacts in New York. The project will include a private "Made in NY" initiative to support the potential purchase of \$400 million in certain tools and equipment from companies around New York State to create, attract, and retain manufacturers and suppliers across the state.

In addition, the companies will support a \$15 million fund to increase the role of minority- and women-owned businesses. These technology developments may facilitate the possibility of building a 450mm plant in New York state. These plants are projected to cost in excess of \$10 billion each.





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