450 mm Equipment Performance Metrics

ISMI Response after Second Supplier Workshop

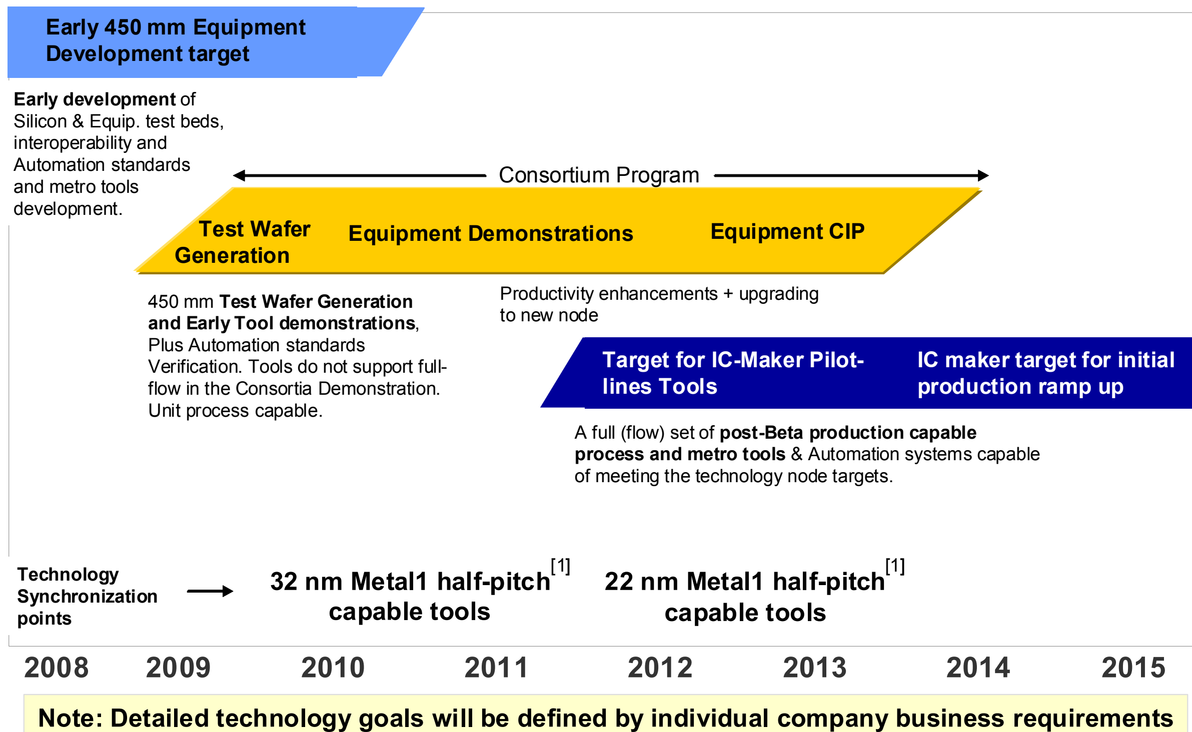
Purpose

This document provides customer targets for process and manufacturing performance to Suppliers as they begin development of 450 mm equipment and look forward to the launch of manufacturing on the larger wafer size. In this second release, the scope expands to include expectations for about half of the tool set; subsequent updates will encompass all wafer fab tools.

Introduction

IC Makers wish to work with Suppliers of wafer fab equipment to achieve capability for pilot lines in 2012 and prepare for manufacturing their products on 450 mm wafers. They have determined that their technology targets for the period coincide quite well with ITRS definitions for contacted metal half pitch at the 32 nm and 22 nm generations.

- The development and demonstration phase, roughly from 2010 to 2012, will focus on 32 nm capability from early testing to first production-worthy process and metrology equipment.
- Equipment maturation thereafter must achieve High Volume Manufacturing (HVM) cost/performance to support production ramp while technology scales to 22 nm and beyond.



[1]: Reference is DRAM stagger-contacted Metal 1 half-pitch in nanometers

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II. General requirements
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I. Applicable Guidelines and Standards

The expectations for 450 mm tools include capabilities and configurations specified in the ISMI Unified 450 mm / Next Generation Factory Guidelines. Included are compliance with SEMI standards currently applicable to 300 mm tools or their equivalents for 450 mm, which may be under development at inception.

- Key is compliance with S2 Safety and S8 Ergonomics standards
- Other examples include the use of 25 Front Opening Unified Pods as the in-fab carrier and the BOLTS standard for interface between E15.1 load ports and Equipment Front End Modules.

In addition, certain improvements, e.g. to FOUP purging and sealing capability, or the extension of standardization to platform / module interfaces may be developed.

The Guidelines, citing applicable standards, are included in these requirements by reference, and may be accessed at www.ismi.sematech.org, and SEMI Standards may be accessed at www.semi.org.

II. General Requirements

The overarching requirement for 450 mm manufacturing is that it maintain the advantageous cost structure that has enabled continuing growth for industry. While no explicit cost metrics are included in this document, this fundamental objective must be recognized in developing 450 mm equipment. The implications of this imperative are significant for all equipment, but for some types, specific elements will be called out in the individual metrics sheet.

A boundary condition is that 450 mm equipment be more productive than its 300 mm predecessor.

- For most equipment the ITRS Factory Integration requirement that productivity improve by 4% per year should be applied to the 300 mm 2009 baseline throughput in wafers per hour for the same tool configuration.
- It is recognized that for area-based tools, such performance will require major innovation and may not be achieved at the first generation; specific metrics and progress rates will be listed for such tool types.

450 mm manufacturing capability must comprehend the re-use of existing 300 mm facilities. The footprints of tools must not increase by more than 10% for a given number of wafers per unit time; the absolute heights of all process and metrology tools must be less than or equal to 12 feet.

Consumables represent a significant cost in manufacturing for many process steps. In general, consumables should be held to the same level for 450 mm as for 300 mm on a per-wafer basis. For some processes, significant reductions are required and will be specified in the individual metrics sheets.

ESH requirements are, broadly, to maintain or reduce the amounts of effluents and the use rates for most chemicals for 450 mm tools relative to the 300 mm 2009 baseline on a per-wafer basis.

- ***It is an absolute requirement that all equipment must be safe to operate and maintain at any stage of maturity.***
- ***Equipment spare parts and modules must either be small and light enough to handle safely during maintenance, and clearances adequate, or ergonomic handling aids must be provided.***

Personal Guided Vehicles (PGVs) will be required at inception for FOUP transport and for loading and unloading of FOUPS on tools.

III. Equipment Performance Metrics by Tool Type

450 mm Process and Metrology Equipment is categorized in the following one-page format by Tool Types, with sections for tool parameters, standards compliance and metrics for example processes and manufacturing performance.

Tool Types (those covered in this revision listed in red)

Tool No.	Tool Type	Tool Description	Process Example
Lithography			
1.1	Exposure	193 nm	Critical levels
1.2	Exposure	193 nm Immersion	Critical levels
1.3	Exposure	248 nm	Non-critical levels
1.4	Track	Coat/develop	All levels
CMP			
2.1	CMP	Dielectric	Contact - Planarize PSG
2.2	CMP	Metal	(1) Contact – Tungsten Plug Polish
2.3	CMP		(2) Damascene - Copper Polish
CVD			

3.1	CVD	PECVD (HPCVD or HARP)	(1) Active Area - STI Fill - Undoped Ox
3.2	CVD		(2) SiN, SiCN Barrier / Etch Stop / Cap
3.3	CVD		(3) Low k Dielectric
3.4	CVD		(4) Contact - Nitride Etch Stop & Liner
3.5	CVD	Metal CVD	(1) Contact – Tungsten Plug
3.6	CVD		(2) Contact – Ti / TiN Barrier for W Plug
3.7	CVD		(3) TaN / Ta Barrier for Cu Metal layers
3.8	CVD		(4) TiN Metal Hard Mask for Damascene Etch
3.9	CVD	ALD	(1) Dielectric
3.10	CVD		(2) High k Dielectric
3.11	CVD		(3) SiGe
3.12	CVD		(4) Tungsten
PVD			
4.1	PVD	PVD-Metal	(1) Gate Metal
4.2	PVD		(2) Silicide Metal
4.3	PVD		(3) Cu Seed
4.4	PVD	Reactive Sputter	(1) Contact – Ti / TiN Barrier for W Plug
4.5	PVD		(2) TaN / Ta Barrier for Cu Metal Layers
4.6	PVD		(3) TiN Metal Hard Mask for Damascene Etch
Dry Etch			
5.1	Dry Etch	Dielectric; Poly	Active Area - STI Trench
5.2	Dry Etch	Dielectric	(1) Gate - Nitride Spacer
5.3	Dry Etch		(2) Contact
5.4	Dry Etch		(3) Via / Damascene Trench
5.5	Dry Etch	Poly	Gate - Polysilicon / ARC
5.6	Dry Etch	Metal	(1) Gate - Metal Electrode
5.7	Dry Etch		(2) Silicide Metal
5.8	Dry Etch		(3) Metal Hard Mask for Damascene
5.9	Dry Etch	Bevel Edge Clean Etch	
Dry Strip			
6.1	Dry Strip	Asher	(1) Active Area
6.2	Dry Strip		(2) Source/Drain Implant
6.3	Dry Strip		(3) Gate Electrode, Silicide, Metal Hard Mask
Electrochemical Plating			
7.1	Electrochemical Plating	Copper	Damascene Fill
Doping			
8.1	Ion Implantation	High Energy	Deep Wells
8.2	Ion Implantation	Medium Current	Gate Extensions
8.3	Implant / Plasma Immersion	Low Energy / High Current	Source / Drain
Thermal Process			
9.1	Thermal Process	Oxidation Vertical Furnace	(1) Active area- Field Oxide
9.2	Thermal Process		(2) Rounding oxidation
9.3	Thermal Process		(3) N-well Sacrificial Oxide
9.4	Thermal Process	Anneal Vertical Furnace	(1) Densification
9.5	Thermal Process		(2) Low Temp Anneal
9.6	Thermal Process	Nitride LPCVD	Gate Spacer
9.7	Thermal Process	Poly LPCVD	Gate Electrode
9.8	Thermal Process	Rapid Thermal Anneal	(1) Silicide
9.9	Thermal Process		(2) Source / Drain Anneal
9.10	Thermal Process	Millisecond Anneal	Source / Drain Anneal
Wet Process (Single Wafer or Batch Process?)			
10.1	Wet Etch	Wet Nitride	Active-area- Oxy-Nitride Strip
10.2	Wet Clean	VP-HF	Active area- Ozone/Anhydrous HF clean
10.3	Wet Clean	Wet Clean	(1) Particle Removal
10.4	Wet Clean		(2) Pre- / Post-Ash
10.5	Wet Clean		(3) Backside Clean
10.6	Wet Clean	Solvent	Solvent Clean
Metrology			
11.1	Bare Wafer Particle		
11.2	Film Thickness		
11.3	CD		
11.4	Overlay		
11.5	Patterned Defect		

How to View the Following Requirements

Each metric is listed by attribute with units and targets for 32 nm and 22nm. Suppliers should target 32 nm capabilities for the 2010-11 demonstration period and plan for extension to 22 nm capability by the 2012-14 piloting phase. Manufacturing metrics are expectations for HVM.

It is recognized that, initially, tools will not be as capable with regard to either process or productivity goals as the metrics presented in this document, and may not comply with all guidelines and standards. They must be safe to operate and maintain.

A general rule is that 450 mm tools must provide process capability equal to or better than the equivalent 300 mm tool at the same technology generation. It is important for Suppliers to view the 32 nm metrics here as generic targets for consortial demonstration and to check with prospective customers on their specific process requirements moving into the 22 nm pilot line phase in order to ensure that proper capability is in place for optimal investment.

> Total variability refers to the statistical combinatiion of all sources of variability; e.g. within-wafer, wafer-to-wafer, run-to-run, station-to-station, expressed in standard deviation as either an absolute number or a percentage of the target for the metric.
>
> Edge exclusion is under study in response to Supplier feedback. ITRS lists it variably as either 1.5 mm or 2 mm for 32 /22 nm technology, depending on the parameter, though current practice at 300 mm is generally higher. We would like to discuss the engineering implications with Suppliers as to the challenges of achieving the tighter goals for 450 mm.

Productivity must also be as good or better than 300 mm for the same tool configuration, manufacturing metrics for 450 mm in this document are meant to be aggressive. All else being equal, opportunity for selection will likely be best for those tools that achieve customer process requirements and maximize productivity.

Note on Metallic Contamination *Preliminary guidance - requirements may be changed for 32 nm and 22 nm as development proceeds*

All metals should generally be present on wafer surfaces after processing at no more than 1E10 atoms per cm^2.   Cr, Fe, Co, Ni, Zn, Mn, Ti Na, K, Mg, Ca, Al, Cu, Au, Ag are examples of metals for which contamination levels will be measured (testing methods will be defined)

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Metrics Definitions

Equipment name – This identifies the equipment type and specific process application, key process parameters, sampling plan, etc.

Equipment parameters – This identifies desired unique equipment features like stepper/scanner field size, electrostatic chuck for vacuum tool applications, integrated or clustered tools, etc.

Throughput – Raw throughput in wafers per hour assuming 100% uptime (continuous, uninterrupted processing, cascade mode, and not depreciated for downtime, setup, etc.). For metrology tools, throughput may be weighted by a sampling plan if specified on the equipment metrics form.

Mean Time Between Failure (MTBF) – Mean productive time to fail as a function of processing time, not clock time. This definition is in line with the SEMI E10-0304 standard.

Mean Time To Repair (MTTR) – This includes qualification test time. This definition is in line with the SEMI E10 standard.

Edge exclusion – Area around the wafer edge that does not receive uniform/reliable processing and will not yield complete electrical circuit.

Note: For purposes of this document, a 1.5 mm edge exclusion is targeted.

Defectivity – *represented by the particle density above a referenced threshold defect size outside the edge exclusion zone.*

- Defect Density is number of particles per unit area, typically per square centimeter.
- PWP - Per Wafer Pass refers to the particles added to the wafer by one cycle through the tool / process.
- For purposes of this document and the early demonstrations of 450 mm equipment, bare wafer defect levels are converted to equivalent density at 30 nm particle size to reflect current detection capability.
    - For reference, if 50 nm defect detection is used, target is adjusted to 40% of the number listed for bare wafer at 30 nm in the metrics sheet.
- Defectivity metrics for each tool may include targets for bare wafer, back side, in-film and/or with-pattern particle densities, as applicable

Process – This is a ***generic*** process that highlights key process criteria for each tool. It is used to develop tool performance data as outlined above and is also intended to be used for 450 mm equipment performance demonstrations. Processes will essentially be the same for 450 mm tools as for 300 mm at a given technology generation.

Factory and Equipment Performance Metrics

Numbering for factory and equipment tables.

Appendix	Revision	Description
1		Lithography
2		CMP
3		CVD
4		PVD
5		Dry Etch
6		Dry Strip
7		Electrochemical Plating
8		Doping
9		Thermal Process
10		Wet Process
11		Metrology
		(future) Personal Guided Vehicle (PGV)
		(future) Load Port/EFEM
		(future) Carriers
		(future) AMHS
		(future) ESH
		(future) Stocker
		(future) Equipment Software
		(future) Factory Automation Software
		(future) FOUP Cleaner
		(future) Wafer Sorter

Document Revision History

Revision	Appendix Revised	Date	Reason For Change
Initial Release		11/18/08	
1.0	All	12/30/08	ISMI Response to 11/18/08 Supplier Workshop
2.0	All	3/31/09	ISMI Response to 2/25/09 Supplier Workshop

Companion Documents

- **Relaxed Initial Expectations for Early Test Wafer Generation Tools**

  To support early development of equipment in 2009 – 2010, certain tools will be required to provide test wafer capability before they are mature enough for demonstration. There are relaxed expectations for their performance at inception and key parameters will be specified through consultation with Suppliers for this starting phase.

  > ***A separate document details these less-stringent expectations of tools needed early for test wafer generation.***

  Performance improvement for test wafer generation must be pursued in parallel as the overall capability of the tools is developed. The expectations for performance during demonstration and production launch for all tools, including those needed at early maturity for test wafer generation, will be included in this document as it is developed in consultation with Suppliers.

Tools Needed Early for Test Wafer Generation

Early Patterning Capability

Oxide Vertical Furnace

PECVD Dielectric

Dielectric Dry Etch

Dielectric CMP

PVD Metal

LPCVD Nitride

Wet Cleans

Dry Strip Asher

Bare Wafer Particle Detection

Thin Film Thickness

CD Measurement

- **Demonstration Test Methods**

  A separate document on Demonstration Test Methods will detail the means to scale targets accouning for equipment maturity and determine statistical sampling for required confidence, as well as the test structures to be used in demonstration testing.

Appendix 1 – Lithography

1.1 Exposure, 193 nm, Critical levels (tsmc needs Immersion @ 22 nm)

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Min. field size (6 inch reticle)	mm x mm	26 x 33	26 x 33	
	Reduction	Ratio	4:1	4:1	
	Reticle size (6 inch reticle)	inch x inch	6 x 6	6 x 6	
	Partial die at wafer edge		patterned	Patterned	
Process Targets	CD Nominal	nm	32	23	
	CD Control (3σ)	nm	< 2.6	Intra<1.0; Inter <1.0	At best focus / best dose; wafer flatness will be specified for demo
	Total overlay, tool to tool, compatibility	nm	< 6.4	< 4	Ave. + 3σ
	Overlay to self	nm	< 3	< 2	May need to be tighter for double patterning
	Dynamic depth of focus, full field ± CD Control	nm	> 150	> 150	
	Resist-sensitivity typical	mJ/Cm²	20–50 mJ/ cm2	20–50 mJ/ cm2	
	Ref. exposure energy	mJ/Cm²	25	25	
Process Characteristics	Evaluation pattern (1) Line / Space	nm	32	23	CD after develop / bake (no trimming)
	Evaluation pattern (2) Isolated Line	nm	21	15	Likely to require double patterning
	Throughput vs. exposure energy	wafer/hr	to be measured	to be measured	Range of doses to to be specified
	Setup time per recipe	Min	to be measured	to be measured	
	CD repeatability across the wafer, multi-width	nm	to be measured	to be measured	
	Overlap DOF parameters	µm	to be measured	to be measured	
Defects, PWP @ 1.5 mm	On bare Si ≥ 30 nm	#/cm²	< 0.0022	< 0.0007	

edge exclusion target review with Suppliers – not final	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required*
	Availability	%	96	96	Bottleneck tool
	MTBF	Hour	> 700	> 700	
	MTTR	Hour	< 29	< 12	

It is recognized that the throughput requirements shown here are aggressive and will require significant design enhancements.

As was the case at 300 mm, productivity improvements are expected to be introduced over the first couple of 450 mm tool generations

Appendix 1 – Lithography

1.4 Track, Coat/Develop

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	ARC		yes	Yes	
	Edge bead removal (EBR)		yes	Yes	
Process Targets	Process resist thickness	nm	50 - 90	35 – 65	
	Coating uniformity total variability (3 σ)	nm	< 2.1	< 2.1	
	Coating uniformity within wafer (3 σ)	nm	< 1.5	< 1.5	
	Coating uniformity wafer to wafer (3 σ)	nm	< 1.5	< 1.5	
	Develop uniformity within wafer (3 σ)	nm	< 5	< 5	
	Develop uniformity total variability (3 σ)	nm	< 4	< 4	
	Develop uniformity wafer to wafer (3 σ)	nm	< 3	< 3	
	Bake uniformity total variability (90–110°C) (3 σ)	°C	< 0.2	< 0.2	
	Bake uniformity total variability (110–150°C) (3 σ)	°C	< 0.3	< 0.3	
	EBR D Radius (3 σ)	mm	< 0.15	< 0.15	
	Photo resist Dispense volume (for saving)	cc/wfr	< 1.0	< 1.0	Needs more evaluation
Process Characteristics	Contact angle after adhesion process	Degree	60–70	60–70	
	NH3 concentration	Ppb	< 1.0	< 1.0	
	EBR D Theta (3 σ) (Optical EBR/Notch Area)	Degree	to be measured	to be measured	
	Life of chemical filter in 50 ppb cleanroom	Months	> 12	> 12	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0013	< 0.001	
	In-film	$\#/cm^2$	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si	$\#/cm^2$	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
	Pattern	$\#/cm^2$	< 0.02 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Must not limit scanner	Must not limit scanner	
	Availability	%	96	96	
	MTBF	Hour	> 700	> 700	Bottleneck tool
	MTTR	Hour	< 29	< 12	
	Wafer transfer failure rate (transfer reliability)			< 1/1000	

Appendix 2 – CMP

2.1 CMP, Dielectric, Contact – Planarize PSG

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto pad condition		required	required	
	In situ thickness monitoring and end point detection		required	required	
	Automated Process Control		required	required	Host communicate incoming uniformity and compensation parameters
	Integration with post – CMP clean		required	required	
	Dry in – Dry out		required	required	
Process Targets	CMP uniformity total variability (3 σ) – all sources	%	< 4	< 4	**Current capability**
	Head-to-head variation in removal rate (3 σ)	%	< 3	< 1.5	
	Dielectric thinning (condition: over-polish 10-20%)	nm	tbd	Tbd	Structure to be specified for demo
Process Characteristics	Rate stability parameters (drift, pad life >500 wafers)	%	< 10	< 5	Must compensate for pad life
	Scratches	/cm²	< 0.1	< 0.1	
	Removal rate	nm/min	**320**	**320**	
	Dishing/over/under erosion on patterned wafers	nm	to be measured	to be measured	
	Slurry Waste	lpm	Per wafer, same as 300 mm or better	Per wafer, same as 300 mm or better*	
	Pad Consumption (use rate on per-platen basis **/ (all platens**)		1200	1200	
Defects, PWP @ 1.5 mm	On bare Si ≥ 30 nm	#/cm²	< 0.0076	< 0.0055	.

edge exclusion target review with Suppliers – not final	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 2	< 2	

* CMP is one of the key processes where consummables cost must be brought down significantly, either with new designs for 450 mm or engineering improvements over time

Appendix 2 – CMP

2.2 CMP, Metal - Tungsten Plug Polish

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto pad conditioner		required	required	
	In situ thickness monitoring and end point detection		required	required	Why in situ thickness monitoring needed for W polish? – Is there an over polish concern driving APC need. Uniformity control specs don't indicate overpolish as a concern
	Automated Process Control		required	required	Host communicate incoming uniformity and compensation parameters
	Integration with post – CMP clean		required	required	
	Dry in – Dry out		required	required	
Process Targets	CMP uniformity total variability (3 σ) – all sources	%	**< 4**	**< 4**	**Current capability**
	Head-to-head variation in removal rate (3 σ)	%	< 3	< 1.5	
	Dielectric thinning (condition: over-polish 10-20%)	nm	tbd	tbd	**Structure to be specified for demo**
Process Characteristics	Rate stability parameters (drift, pad life >500 wafers)	%	< 10	< 5	Must compensate for pad life
	Scratches	/cm²	< 0.1	< 0.1	
	Removal rate	nm/min	**300**	**300**	Rate is very high vs. 300 mm rate – propose 300nm/min as target **(agree - was 500)**
	Dishing/over/under erosion on patterned wafers	nm	to be measured	to be measured	
	Slurry Waste	lpm	Per wafer, same as 300 mm or better	Per wafer, same as 300 mm or better*	
	Pad Consumption (use rate on per-platen basis / **all platens**)	Wafers/pad	> 1200	> 1200	On which platen? Is this driven by Availability and are we concerned with cost of ownership. Pad and Slurry development will needed.

Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0087	< 0.0062	Need bevel shape specified and film thickness need to be specified for meeting edge exclusion... **450mm bevel details not known today**
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 2	< 2	

* CMP is one of the key processes where the cost of down time and consummables must be brought down significantly, either with new designs for 450 mm or engineering improvements over time

Appendix 3 – CVD

3.1 CVD, PECVD - STI Fill / Undoped Ox

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness	nm	350	350	Process specific
	Film thickness uniformity total variability (3σ)	%	< 3	< 3	Thickness dependent
	Stress (compressive)	Mpa	> 150 and < 250	> 150 and < 250	Process specific
Process Characteristics	Film shrinkage	%	to be measured	to be measured	
	Step coverage	%	95	95	
	Refractive Index (RI)		to be measured	to be measured	
	Plasma charge damage		to be measured	to be measured	**Testing to be defined**
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0068	< 0.0042	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si **measure, improve to best possible, discuss redesigns needed to meet**	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 8	< 4	

Appendix 3 – CVD

3.3 CVD, Dielectric – Low k Dielectric

Note: Specialized processing techniques other than thermal CVD may be required for these films.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness	nm	350	350	Process specific (why not provide thickness range)? **Demo thickness**
	Film thickness uniformity total variability (3 σ)	%	< 3	< 3	Thickness dependent
	Stress	MPa	**To be measured**	**To be measured**	Process specific – is it a wish for this to be compressive or a need. **Check with Customer**
Process Characteristics	Film shrinkage	%	**< 4**	**2 GPa**	Is this need or target? Depends on K value. **Loosened from 1%**
	Step coverage **Needed for planarized back end?**	%	95	95	Why is 95% step coverage required is this for backend?
	Refractive Index (RI)		to be measured	to be measured	
	V_{BD}		**8MV/cm**	**8MV/cm**	
	Film hardness		**2 GPa**	**2 GPa**	
	Plasma charge damage **Testing to be defined**		to be measured **It can be a problem for advanced process**	to be measured **It can be a problem for advanced process**	Historically not worried about plasma damage for backend. Is this something industry sees a problem.
Defects, PWP @ 1.5 mm	On bare Si ≥ 30 nm	#/cm^2	< 0.0068	< 0.0049	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	

edge exclusion target review with Suppliers – not final	Backside on Si **– measure, improve to best possible, discuss redesigns needed to meet**	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	Is target to get rid of backside cleans – these type of targets are high for CVD and would require significant redesign
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 8	< 4	

Appendix 3 – CVD

3.5 CVD, Metal – Contact Tungsten Plug

Note: this process may require specialized deposition techniques in addition to CVD to initiate deposition at these dimensions

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness	nm	350	350	Process specific
	Film thickness uniformity total variability (3 σ)	%	< 3	< 3	Thickness dependent
	Stress (compressive)	MPa	> 150 and < 250	> 150 and < 250	Process specific
	Contact size	nm	36	25	
	Aspect ratio	H/D	10:1	14:1	
Process Characteristics	Film shrinkage	%	to be measured	to be measured	
	Step coverage	%	95	95	
	Plasma charge damage		to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0041	< 0.0029	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 10	< 6	

Appendix 4– PVD

4.1 PVD, Gate Metal

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Comments
Equipment Parameters	Wafer temperature range	°C	25–500	25–500	
	Base vacuum @ 250°C	Torr	< 1.00 E-8	< 1.00 E-8	
	Pre clean function required		Yes	yes	
Process Targets **Material / stack parameters to be specified for demo**	Metal A thickness	nm			Process specific
	Metal B thickness	nm			Process specific
	Pre clean oxide etch uniformity total variability (3 σ)	%	< 2	< 2	Thickness dependent
	Film thickness uniformity total variaiblity (3 σ)	%	< 2	< 2	Thickness dependent
	Pre clean charge up damage		None	None	
Process Characteristics **Material / stack parameters to be specified for demo**	Metal A resistivity	μOhm – cm	to be measured	to be measured	
	Metal B resistivity	μOhm – cm	to be measured	to be measured	
	Metal A stress	Pa	to be measured	to be measured	
	Metal B stress	Pa	to be measured	to be measured	
	Sidewall coverage parameters	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0047	< 0.0034	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 700	> 700	
	MTTR	Hour	< 8	< 4	

Appendix 4– PVD

4.4 PVD, Reactive Sputter Ti / TiN Barrier for Tungsten Plug

Note: these films may require processes other than PVD to achieve required conformality at 32 nm and 22 nm.

We will provide additional guidance as development proceeds

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Comments
Equipment Parameters	Wafer temperature range	°C	25–350	25–350	
	Base vacuum @ 250°C	Torr	< 1.00 E-8	< 1.00 E-8	
	Pre clean function required		Yes	yes	
Process Targets	Ti thickness	nm	15	15	Process specific
	TiN thickness	nm	30	30	Process specific
	Pre clean oxide etch uniformity total variability (3 σ)	%	< 2	< 2	Thickness dependent
	Film thickness uniformity total variaiblity (3 σ)	%	< 2	< 2	Thickness dependent
	Aspect Ratio	H:D	10:1	14:1	
	Ti/TiN bottom coverage (logic)	%	> 80	> 80	
	Pre clean charge up damage		None	None	
Process Characteristics	Ti resistivity	µOhm – cm	to be measured	to be measured	
	TiN resistivity	µOhm – cm	to be measured	to be measured	
	Ti stress	Pa	< 1.00E+9	< 1.00E+9	
	TiN stress	Pa	to be measured	to be measured	
	Sidewall coverage parameters	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0047	< 0.0034	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 700	> 700	
	MTTR	Hour	< 8	< 4	

Appendix 4– PVD

4.5 PVD, Reactive Sputter TaN / Ta Barrier for Cu Metal Layers

Note: these films may require processes other than PVD to achieve required conformality at 32 nm and 22 nm.

We will provide additional guidance as development proceeds

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Comments
Equipment Parameters	Wafer temperature range	°C	25–500	25–500	
	Base vacuum @ 250°C	Torr	< 1.00 E-8	< 1.00 E-8	
	Pre clean function required		yes	yes	
Process Targets	Ta thickness	nm	TBD	TBD	
	TaN thickness	nm	TBD	TBD	
	Pre clean oxide etch uniformity total variability (3 σ)	%	< 3	< 2	
	Film thickness uniformity total variaiblity (3 σ)	%	< 3	< 2	
	Ta/TaN bottom coverage (logic)	%	> 20	> 20	
	Pre clean charge up damage		None	None	
Process Characteristics	Ta resistivity	μW – cm	to be measured	to be measured	
	Ta stress	Pa	to be measured	to be measured	
	TaN stress	Pa	to be measured	to be measured	
	Sidewall coverage parameters	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0047	< 0.0034	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	96	96	
	MTBF	hour	> 700	> 700	
	MTTR	hour	< 8	< 4	

Appendix 5 – Dry Etch

5.2 Dry Etch, Gate Nitride Spacer

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto End-point Detection	-	Required	Required	
	Bevel Defect Detection		Option	Option	*in-situ* not required / stand-alone OK Need better solution to eliminate bevel polymer contamination
	In-situ Chamber Clean	-	Required	Required	
Process Targets	CD after Etch	nm	13	9	**Material / structure to be specifeid for demo**
	Total Variability 3 σ – all sources	nm	< 0.64	< 0.44	
Process Characteristics	Selectivity to	-	> TBD , each company input selectivity requirements w.r.t materials chosen	> TBD, each company input selectivity requirements w.r.t materials chosen	**Check with customer**
	Loading Effect	%	< 5	< 5	Etch rate difference I/s to iso **Structure to be specified for demo**
	Charge Damage	-	To be measured	To be measured	
	Residue after etch	-	None	None	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0092	< 0.0066	Need to find better solution for e-chuck to eliminate need for post-etch backside clean
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 350	> 350	
	MTTR	Hour	< 8	< 3	
	MTB/T Clean		To be measured	To be measured	Will depend on process chemistry

1. Need to specify uniformity requirements, such as thickness remaining and selectivity targets.
2. Loading effect should specify wafer center vs edge; variation with line width

5.3 Dry Etch, Dielectric, Contact

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto End-point Detection	-	Required	Required	
	in-situ Bevel Defect Detection		Required	Required	Need better solution to eliminate bevel polymer contamination
	In-situ Chamber Clean	-	Required	Required	
Process Targets	Contact CD at Resist	nm	39	28	
	Contact CD after Etch	nm	36	25	
	Aspect Ratio	H:D	> 10:1	> 14:1	
	Total Variability 3 σ – all sources	nm	< 1.5	< 1	
Process Characteristics	Selectivity to	-	> TBD , each company input selectivity requirements w.r.t materials chosen	> TBD, each company input selectivity requirements w.r.t materials chosen	
	Loading Effect	%	< 5	< 5	Etch rate difference l/s to iso
	Charge Damage	-	To be measured	To be measured	
	Residue after etch	-	None	None	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0084	< 0.0060	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	Need to find better solution for e-chuck to eliminate need for post-etch backside clean
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 350	> 350	
	MTTR	hour	< 8	< 3	
	MTB/T Clean		To be measured	To be measured	Will depend on process chemistry

Appendix 5 – Dry Etch

5.6 Dry Etch, Gate Metal Electrode

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto End-point Detection	-	Required	Required	
	Bevel Defect Detection		Option	Option	*in-situ* not required / stand-alone OK Need better solution to eliminate bevel polymer contamination
	In-situ Chamber Clean	-	Required	Required	
Process Targets **Material / stack parameters to be specified for demo**	CD at Resist	nm	21	15	MPU, DRAM based on ITRS etch bias
	CD after Etch	nm	13	9	MPU, DRAM Physical Gate Length
	Total Variability 3 σ – all sources	nm	< 0.64	< 0.44	
Process Characteristics	Selectivity to	-	> TBD , each company input selectivity requirements w.r.t materials chosen	> TBD, each company input selectivity requirements w.r.t materials chosen	**Check with customer**
	Loading Effect	%	< 5	< 5	Etch rate difference I/s to iso
	Charge Damage	-	To be measured	To be measured	**Testing to be defined for demo**
	Residue after etch	-	None	None	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0092	< 0.0066	Need to find better solution for e-chuck to eliminate need for post-etch backside clean
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 350	> 350	
	MTTR	Hour	< 8	< 3	
	MTB/T Clean		To be measured	To be measured	Will depend on process chemistry

1. Need to define Gate metal electrode structure (a generic one is fine) **Yes**
2. CD after etch **Yes - at resist (ADI) based on ITRS etch bias**
3. Can sputter etch acceptable? **No**
4. Contamination measurement method and metrology, need to define a common agreeable method. **Test method to be specified**

5. What is the wafer edge exclusion? Final?
6. Add specification for what metrology will be used to measure total varaiblity for gate metal electrode **Test method to be specified**
7. Ensure that metro spec for measuring gate metal electrode is equivalent in related metrology EPM set. **Yes**
8. HHT: cannot comment on validity of gate metal etch without knowing materials (which are not specified in EPM) **(demo testing to be specified) – check with customer**
9. For demonstration – we will need to define a basic enough gate structure and metals which all can agree upon to get agreement/commitment to EPM's for this tool **Yes**
10. Input is that material and stack will be important, and sooner we can share this it will be valuable. Does not have to be a specific material, can be a range. **Yes**
11. Residue after etch is highly dependant on metal stack, so ability to judge if spec can be met will be dependant on the stack. **Yes**
12. Can ISMI agree on the methodology for measuring metallic contamination (TRXF, Vapor Phase, etc) ? **Test method to be specified**
13. Need to better understand better the productivity requirements for 450mm systems (eg throughput, relative footprint) **Such global requirements coming in EPM 3**
14. Does total variability – all sources mean wafer to wafer or within wafer ? Chamber matching and wafer to wafer requirements are missing – particularly for gate – first we need to decide if chamber matching is really part of the demo scope ? **See explanation of total variability in EPM text. Chamber match beyond scope of demo – will need to meet same req as 300 mm**
15. Additional concern expressed about viability of 1.5mm edge exclusion as related to ability to find better solution for e-chuck
16. Additional metrics requested – **Check with customer To be measured (test structure and method to be specified)**
    a. Gate Profile requirements information ??
    b. Etch rate uniformity spec ? If you go to 3D-type structures, gate is specififed by etch rate and not CD
    c. Line edge roughness spec ?

Appendix **5**– Dry **Etch**

5.9 Bevel Edge **Etch**

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto endpoint		None	None	
	Cathode temperature controller		Required	Required	
	Vision (Bevel Etch Confirm)		Required	Required	
	Laser Sensor (Gap Check)		Required	Required	
Process Targets	Oxide Etch Rate	A/min	> 20000	> 20000	
	Poly Etch Rate	A/min	>20000	>20000	
	Uniformity within wafer (3 σ)	%			
	Uniformity wafer to wafer (3 σ)	%	< 5	< 5	
	Polymer residue		None	None	
	Etched material redeposition		None	None	
Process Characteristics	Charge up damage Testing to be defined		To be measured	To be measured	
Defects, PWP @ 1.5 mm edge exclusion target review with Suppliers – not final	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0028	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 900	> 900	
	MTTR	Hour	< 8	<3	

1. The Bevel edge clean needs a new EPM table, the current one is just like a Bulk strip tool requirement **Yes, new chart**
   a. is it a (1) Post-etch Bevel etch; (2) Clean at the top; (3) Deep bevel edge clean or others?
   b. Need to specify as 'post etch bevel edge clean' , or post deposition bevel edge clean' to be more clear.
   c. Nothing really related to classical bevel edge clean (specifically temperature control, it indicates some kind of an asher process). Need more clarification on it is really a bump stripper or a bevel stripper – and why is it plasma limited, or can it be wet process ?

2. If only cleaning the bevel, why concerned about oxide loss ?
3. What is the re-deposition requirement **Zero**
4. Ashing rate?
5. What is really needed: **Will consider**
    a. Undercut
    b. Concentricity – and cleanliness of bevel all the way around.
    c. General cleans or also backside etch in addition to bevel process.

Appendix 6 – Dry Strip

6.1 Dry Photoresist Strip, Asher

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto endpoint Wafer temperature controller		Required Required	Required Required	
Process Targets	Ashing rate Ashing rate uniformity within wafer (3 σ) Ashing rate uniformity wafer to wafer (3 σ) Selectivity to all but resist Oxide loss (implanted)	µm/min % % Ratio Nm	> 10 < 5 < 5 > 500 < 0.1	> 10 < 5 < 5 > 500 < 0.1	
	Silicon loss	Nm	< 0.1	< 0.1	
Process Characteristics	Charge up damage **Testing to be defined** CV shift Residue after ashing detectable by dark field microscope or defect tool haze indication Temperature control to	mV deg – C	None to be measured None 350 +/- 10	None to be measured None 350 +/- 10	Process dependent
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm Backside on Si	#/cm^2 #/cm^2	< 0.0038 < 0.28 @ ≥ 75 nm	< 0.0028 < 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability MTBF MTTR	% Hour Hour	95 > 900 < 8	95 > 900 <3	

Appendix 7 – Electrochemical Plating

7.1 Cu Plating (700 nm Cu Film)

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness total variability (3 σ) Resistivity Trench size/via size Contact fill (single damascene at < 40 nm trench)	% µOhm-cm nm aspect ratio	< 3 < 1.8 43 / 36 6	< 3 < 1.8 30 / 25 6	< 1.8µ Ω -- cm @ 1µ m (anneal@100C,60min)
Process Characteristics	Film stress Void formation Grain size		to be measured Free to be measured	to be measured Free to be measured	< 120MPa @ 1µ m
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm Backside on Si	#/cm² #/cm²	< 0.0021 < 0.28 @ ≥ 75 nm	< 0.0015 < 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability MTBF MTTR	% hour hour	95 >500 < 4	95 >500 < 4	

Appendix 8 – Doping

8.1 Ion Implantation: High Energy

.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment mechanical wafer throughput	wafer/hr	230	230	
Process Targets	Energy range Max (single charge)	keV	3000	3000	
	Energy range Min (single charge)	keV	10	10	
	Dose range Max	Ion/cm²	1.00E+15	1.00E+15	
	Dose range Min	Ion/cm²	1.00E+10	1.00E+10	
	Dose uniformity total variability (3 σ)	%	< 1.3	< 1.3	
	Dose uniformity within wafer (3 σ)	%	< 1.3	< 1.3	
	Dose uniformity wafer to wafer (3 σ)	%	< 1.3	< 1.3	
	Dose repeatability total variability (3 σ)	%	2	2	
	wafer to wafer (3 σ)	%	1.3	1.3	
	Dose repeatability within wafer (3 σ)	%	1.3	1.3	
	Mass resolution	M/DM	> 60	> 60	
Process Characteristics	Dose purity parameters measured (SIMS)	%	< 0.5	< 0.5	
	Cross contamination	%	< 0.1	< 0.1	
	Beam current parameters		to be measured	to be measured	
	Beam set-up: solid source (hot start)	min	< 10	< 4	
	Wafer temperature As+, maximum beam current	°C	60	60	
	Beam stability glitch 5 keV ~ max energy	#/ hour	< 5	< 5	
	Beam stability fluctuation 5 keV ~ max energy	%	< ± 5	< ± 1	
	Beam stability parallelism 5 keV ~ max energy	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0027	< 0.0020	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required
	Availability	%	96	96	Bottleneck tool

Phase)	MTBF	hour	> 250	> 250	
	MTTR	hour	< 10	< 10	

Appendix 8 – Doping

8.2 Ion Implantation: Medium Current

.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment mechanical wafer throughput	wafer/hr	500	500	
Process Targets	Energy range Max (single charge)	keV	250	250	
	Energy range Min (single charge)	keV	5	5	
	Dose range Max	Ion/cm²	1.00E+15	1.00E+15	
	Dose range Min	Ion/cm²	1.00E+10	1.00E+10	
	Dose uniformity total variability (3 σ)	%	< 1.0	< 1.0	
	Dose uniformity within wafer (3 σ)	%	< 1.0	< 1.0	
	Dose uniformity wafer to wafer (3 σ)	%	< 1.0	< 1.0	
	Dose repeatability total variability (3 σ)	%	2	2	
	Dose repeatability wafer to wafer (3 σ)	%	1.3	1.3	
	Dose repeatability within wafer (3 σ)	%	1.3	1.3	
	Mass resolution	M/DM	> 60	> 60	
Process Characteristics	Dose purity parameters measured (SIMS)	%	< 0.5	< 0.5	
	Cross contamination	%	< 0.1	< 0.1	
	Beam current parameters		to be measured	to be measured	
	Beam set-up: solid source (hot start)	min	< 10	< 4	
	Wafer temperature As+, maximum beam current	°C	60	60	
	Beam stability glitch 5 keV ~ max energy	#/ hour	< 5	< 5	
	Beam stability fluctuation 5 keV ~ max energy	%	< ± 5	< ± 1	
	Beam stability parallelism 5 keV ~ max energy	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0027	< 0.0020	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required
(@ High Volume Manufacturing	Availability	%	96	96	Bottleneck tool

Phase)	MTBF	Hour	> 250	> 250	
	MTTR	Hour	< 10	< 10	

Appendix 8 – Doping

8.3 Doping: Low Energy / High Current

Tool architecture is not specified; process technology other than ion implantation may be required for ultra-shallow high dose doping

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment mechanical wafer throughput	wafer/hr	200	200	
Process Targets	Energy range Max	keV	120	120	
	Energy range Min for future ultra-shallow junction	keV	0.1	0.1	
	Dose range Max	Ion/cm^2	1.00E+16	1.00E+16	
	Dose range Min	Ion/cm^2	1.00E+11	1.00E+11	
	Dose uniformity total variability (3 σ)	%	< 1.0	< 1.0	
	Dose uniformity within wafer (3 σ)	%	< 1.0	< 1.0	
	Dose uniformity wafer to wafer (3 σ)	%	< 1.0	< 1.0	
	Dose repeatability total variability (3 σ)	%	2	2	
	Dose repeatability wafer to wafer (3 σ)	%	1.3	1.3	
	Dose repeatability within wafer (3 σ)	%	1.3	1.3	
	Mass resolution	M/DM	> 60	> 60	
Process Characteristics	Dose purity parameters measured (SIMS)	%	< 0.5	< 0.5	
	Cross contamination	%	< 0.1	< 0.1	
	Beam current parameters		to be measured	to be measured	
	Beam set-up: solid source (hot start)	min	< 10	< 4	
	Wafer temperature As+, maximum beam current	°C	60	60	
	Beam stability glitch 5 keV ~ max energy	#/ hour	< 5	< 5	
	Beam stability fluctuation 5 keV ~ max energy	%	< ± 5	< ± 1	
	Beam stability parallelism 5 keV ~ max energy	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0030	< 0.0022	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required
	Availability	%	96	96	Bottleneck tool

Phase)	MTBF	Hour	> 250	> 250	
	MTTR	Hour	< 10	< 10	

Appendix 9 – Thermal Process

For thermal processing, key equipment metrics are productivity and and cost of ownership. Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

9.1 Thermal Process, Oxidation Vertical Furnace

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Target oxide thickness	nm	45	45	
	Oxide thickness uniformity total variability (3 σ)	%	2	2	
Process Characteristics	Slip-free process at maximum temperature	°C	950	950	
	Residual oxygen concentration (400–1000°C)	ppb	To be measured	To be measured	See note below
	Spontaneous oxide thickness (400°C, N2)	nm	To be measured	To be measured	See note below
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0022	< 0.0016	
	Backside on Si	$\#/cm^2$	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 6	< 4	

Note: Oxygen concentration will be measured in the process chamber under purge conditions through this temperature range; thickness of any oxide grown on a bare Si wafer pushed and pulled under these conditions will be measured

Work with ISMI and customers to understand batch size constraints given ceiling height maximum

Appendix 9 – Thermal Process

For thermal processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.
Follow-up on relaibility goals

9.4 Thermal Process, Anneal Vertical Furnace EPM 1: 1.5 mm EE a challenge for ThOx (edge th. profile – discuss larger 3-5 mm?)

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	**Temperature range**	**°C**	**400 - 1100**	**400 – 1100**	400 - 1100
	Temperature control	**°C**	**+/- 0.5**	**+/- 0.5**	+/- 0.5
Process Characteristics	Slip-free process at maximum temperature	°C	1100	1100	
	Residual oxygen concentration (400–1100°C)	ppb	To be measured	To be measured	See note below
	Spontaneous oxide thickness (400°C, N2)	nm	To be measured	To be measured	See note below
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0022	< 0.0016	
	Backside on Si	$\#/cm^2$	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 1000	> 1000	
	MTTR	Hour	< 10	< 4	Difficult for batch

Note: Oxygen concentration will be measured in the process chamber under purge conditions through this temperature range; thickness of any oxide grown on a bare Si wafer pushed and pulled under these conditions will be measured

Some customers asking for larger batch size, and even at same batch, will be challenging to stay below 12 feet (10 mm pitch @ 450 mm vs. <10 @ 300 mm) – across all batch thermal tools **Work with ISMI and customers to understand batch size constraints given ceiling height maximum**

9.6 Thermal Process, Nitride LPCVD, Gate Spacer

For thermal processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness Total variability (3 sigma) Step Coverage Process Temperature	nm % % deg-C	40 < + 2 > 90 < 400	35 < + 2 > 90 < 400	Conformal
Process Characteristics	Stress (as deposited) Refractive index / variability Supplier specify process to achieve film	MPa	< 100 To be measured	< 100 To be measured	Structure to be specified for demo
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm In-film Backside on Si	$\#/cm^2$ $\#/cm^2$ $\#/cm^2$	< 0.0038 < 0.01 @ ≥ 20 nm < 0.28 @ ≥ 75 nm	< 0.0028 < 0.01 @ ≥ 10 nm < 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability MTBF MTTR	% hour hour	95 > 300 < 10	95 > 300 < 4	

Work with ISMI and customers to understand batch size constraints given ceiling height maximum

Appendix 9 – Thermal Process

For thermal processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

9.8 Thermal Process, Rapid Thermal Anneal – Silicide   Supplier: can deliver 300 mm-equivalent performance at 450 mm

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Ramp-up Speed (RT – 300°C) for Ni silicide first anneal only	°C / sec	**> 100**	**> 100**	Top temp? ms range
	Temperature uniformity total variability (3 σ at 300°C)	%	< 1	< 1	
	Center-to-edge variation through ramp range	%	< 2	< 2	
Process Characteristics	Ramp-down Speed (300°C to RT)		To be measured	To be measured	
	Overshoot (RT - 300°C)	°C	< 5	< 5	
	Settling Time (RT - 300°C) to within 1% of setpoint	sec	< 1	< 1	
	Slip-free process at maximum temperature	°C	950	950	
	Residual oxygen concentration (200-300°C)	pp**m**	To be measured	To be measured	See note below
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0016	< 0.0012	Challenging **yes**
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	**600+**	> 1000 **Target – if 600 now…**	Batch /**SW**? 500-600 typ
	MTTR	Hour	< 6	< 4	

Note: Oxygen concentration will be measured in the process chamber under purge conditions through this temperature range; thickness of any oxide grown on a bare Si wafer processed under these conditions will be measured   ppm is typical

Appendix 10 – Wet Processes

For wet cleans processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

10.1 Wet Clean, Active Area Oxi-Nitride Removal

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	**Low surface tension solvent drying that leaves no water mark**		yes	yes	
	50:1 HF temperature control (RT)	°C	< + / - 0.1	< + / - 0.1	
	H3PO4 temperature control (160°C)	°C	< + / - 1	< + / - 1	
	HF chemical concentration control	%Wt	**< + / - 0.05**	**< + / - 0.05**	**Current capability**
	H3PO4 chemical concentration control	%Wt	< + / - 1.5	< + / - 1.5	
Process Targets	Silicon Nitride etch rate	A / min	60	60	
	Silicon Oxide etch rate	A / min	1	1	
	Etch uniformity total variability (3σ)	%	< 2.5	< 1.5	
	Water marks	count	none	None	
	Pattern Damage	Count	none	None	Test structure to be defined for demo
	Oxide Loss per Clean Pass	A	none	None	
Process Characteristics	Process time reproducibility **Batch tool** (10 runs 3σ)	sec	< 1	< 1	Process time only
	for process time shorter than 1 min	%	< 0.5	< 0.5	
	Process time reproducibility (10 runs 3σ) Single wafer tool	**sec**	**< 0.5**	**0.5**	Process time only
	Wafer transport time reproducibility (10 runs 3σ) Batch tool	sec	**< 5**	**< 5**	robotic elements
	Wafer transport time reproducibility (10 runs 3σ) **Single wafer tool**	sec	**< 1**	**< 1**	robotic elements
	Time for exchange of chemical in bath	Min	< 1.5	< 1.5	
Defects, PWP @ 1.5 mm	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0027	

edge exclusion target review with Suppliers – not final	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability MTBF MTTR	% Hour Hour	95 **> 700** **< 2**	95 **> 700** **< 2**	**Current capability**

NOTE: Ultrapure chemcals must be used to meet contamination requirements

1. The IPA clean requirement should be replaced by **"Low surface tension solvent clean that leaves no water mark."**
2. Target application
3. Chemical used should meet the same metal contamination level
4. Wafer transport time reproducability – we need to be be more specific on the time between what activities ? Or, call out a uniformity or etch rate specifications if this is the point for the transport time requirement. **Will provide details**.
5. What is the targeted film thickness for this demo ? Is this for thick nitride etching ? **Test structure to be defined for demo**
6. Missing: Selectivities **TBD**

For wet cleans processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

10.3 Wet Cleans, Particle Removal

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Low surface tension solvent drying that leaves no water mark		yes	yes	
	HF temperature control (ambient)	°C	< ± 0.2	< ± 0.2	
	SCx temperature control (22-80°C)	°C	< ± 0.5	< ± 0.5	
	HF Chemical concentration control	%Wt	**< + / - 0.05**	**< + / - 0.05**	**Current capability**
	SCx Chemical concentration control	%Wt	< ± 5	< ± 2	
Process Targets	HF etch uniformity total variability (3σ)	%	< 2.5	< 1.5	
	0.17 µm Particle Removal Efficiency (Si_3N_4) (particles added by dipping, limit is 1,000~10,000)	%	> 95	> 95	
	Water marks (HF last)	count	none	None	
	Pattern Damage	count	none	none	Test structure to be defined for demo
	Silicon Loss per Clean Pass	Ang	0.3 Ang	0.2	
	Particle Removal Efficiency (PRE) on bare wafer	%	90% ≥ 30 nm	90% ≥ 30 nm	Nitride particle on Oxide surface
	PRE with no pattern damage on wafer with 30 nm trench		70%	70%	
	Backside Clean Efficiency	%	85% ≥ 65 nm	85% ≥ 65 nm	
	Residue after SPM/APM detectable by dark field microscope or defect tool haze indication		None	None	
Process Characteristics	Breakdown Voltage	V	to be measured	to be measured	Process specific
	TDDB	sec	to be measured	to be measured	Process specific

	Process time reproducibility Batch tool (10 runs 3σ)	sec	< 1	< 1	Process time only
	for process time shorter than 1 min	%	< 0.5	< 0.5	
	Process time reproducibility (10 runs 3σ) Single wafer tool	sec	< 0.5	0.5	Process time only
	Wafer transport time reproducibility (10 runs 3σ) Batch tool	sec	< 5	< 5	robotic elements
	Wafer transport time reproducibility (10 runs 3σ) Single wafer tool	sec	< 1	< 1	robotic elements
	Time for exchange of chemical in bath	min	< 1.5	< 1.5	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0027	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	**> 700**	**> 700**	
	MTTR	hour	**< 2**	**< 2**	

NOTE: Ultrapure chemcals must be used to meet contamination requirements

Appendix 10 – Wet Processes

For wet cleans processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

10.6 Solvent Clean Removal of Photoresist **Post-Ash Residue**

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Post-clean drying of wafers consistent with clean process		Required	Required	
Process Targets	Solvent clean capable of removing photoresist hardened / crusted by exposure to prior processing at high energies (e.g. reactive ion etch, ion implant…) to the point of allowing complete subsequent cleaning in oxygen plasma		Supplier to specify materials and process parameters to achieve desired result	Supplier to specify materials and process parameters to achieve desired result	
	Temperature control RT – 40°C	°C	< 0.5	< 0.5	
Process Characteristics	Pattern Damage		none	none	
	Process time reproducibility Batch tool (10 runs 3σ)	sec	< 1	< 1	Process time only
	for process time shorter than 1 min	%	< 0.5	< 0.5	
	Process time reproducibility (10 runs 3σ) Single wafer tool	sec	< 0.5	0.5	Process time only
	Wafer transport time reproducibility (10 runs 3σ) Batch tool	sec	< 5	< 5	Robotic elements
	Wafer transport time reproducibility (10 runs 3σ) Single wafer tool	sec	< 1	< 1	Robotic elements
	Time for exchange of solvent in bath	Min	< 1.5	< 1.5	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0027	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing					

Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 1000	> 1000	
	MTTR	Hour	< 6	< 4	

NOTE: Ultrapure chemcals must be used top meet contamination requirements

1. Is it for pre-ash? **Post ashing**
2. Can use H2SO4 + H2O2 / the resist strip tool should also consider SPM tool

Appendix 11 – Metrology

11.1 Bare Wafer Particle

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment Integration with inspection SEM		capable	capable	
	Ability to mask prealignment laser marks		capable	capable	
	Automatic detect classification (in line binning)		capable	capable	
	Ability to perform map difference analysis		capable	capable	
	Communications software/networkability capability		capable	Capable	
Process Targets	Particle sensitivity @ 90% capture rate	nm	30	30	
	Defect size range	nm	30 - 10000	30 - 10000	
	Total count reproducibility (3 sigma) using 30 nm sphere at > 100 count	%	< 2	< 2	
	Coordinate accuracy (repeatability, 3 sigma)	µm	< 5	< 5	
	Absolute coordinate accuracy (newly added)	µm	< 10	< 10	
	Tool-to-tool matching	%	< 3	< 3	
	Precison to Tolerance (P/T) Ratio by size	%	< 15	< 15	
Process Characteristics	Haze sensitivity parameters	ppm	to be measured	to be measured	
	Haze to dynamic range relationship		to be measured	to be measured	
	Edge exclusion	mm	1.5	1.5	
Defects, PWP @ 1.5 nm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.003	< 0.0022	
	Backside on Si	$\#/cm^2$	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	
	Availability	%	98	98	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 20	< 20	

It is recognized that the throughput requirements shown here are aggressive and will require significant design enhancements.

As was the case at 300 mm, productivity improvements are expected to be introduced over the first couple of 450 mm tool generations

Appendix 11 – Metrology

11.2 Film Thickness

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Ability to measure thickness, refractive index, & extinction coeff., reflectivity (RI @ 633, 248, 193 nm)		yes	Yes	
	Ability to measure film stack (RI @ 633, 248, 193 nm)		yes	Yes	
	Reproducibility (Total, 3 σ) site with pattern recognition and 30 µm x 30 µm test site without pattern recognition (RI @ 633, 248, 193 nm)		yes	Yes	
Process Targets	Coordinate accuracy allows "systematic coordinate information" (3σ)	µm	< 1.5	< 1.5	
	Tool to tool matching T, n, K (single layer) (1% total error budget) > 100A	%	< 0.5	< 0.5	
	Tool to tool matching < 100 A		0.2	0.1	
	For 25 nm gate oxide	%	< 0.05	< 0.05	
	Pattern recognition errors (all layers)	%	< 0.01	< 0.01	
	Thickness range (oxide)	Å	5–200 K	5–200 K	
	P/T T = ± 10% when mean thickness < 30 Å T = ± 5% when 30 Å < mean thickness < 1K Å T = ± 1% when 1K Å < mean thickness < 100K Å	%	<10	<10	
Process Characteristics	Accuracy (mean) to be within total uncertainty of standard (Oxide NIST sample)	nm	to be measured	to be measured	
	Result of 30 time repeated test:				
	Accuracy (mean value) : < 10 nm	Å	± 0.5	± 0.5	
	: < 1 µm	Å	± 1	± 1	
	Repeatability : < 10 nm	Å	0.2	0.2	
	: < 1 µm	Å	0.25	0.25	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0022	< 0.0016	
	Backside on Si	#/cm^2	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	98	98	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 20	< 20	

11.3 CD

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Automated SEM		yes	Yes	
Process Targets	CD range	nm	40–5000	40–5000	
	Cd tolerance (reference only) Si etching L/S pattern, 260 nm Pitch	nm	< 3	< 3	
	Reproducibility over one month (3σ) Si etching L/S pattern, 130 nm Line and 260 nm Pitch	%	< 1.5	< 1.5	
	Pattern recognition failure rate (all layers)	%	< 0.05	< 0.05	
	Tool-to-tool matching Si etching L/S pattern, 130 nm Line	%	< 0.5	< 0.5	
	Process/Tolerance	%	< 20	< 20	
Process Characteristics	CD Accuracy (mean) to be within total uncertainty of standard		to be measured	to be measured	
	Charging effect over 30 seconds		to be measured	to be measured	
	Contamination effect after 50 measurements		to be measured	to be measured	
	Contact resolution (top and bottom) 150 nm and 180 nm		to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0026	< 0.0019	
	Backside on Si	$\#/cm^2$	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	98	98	
	MTBF	hour	> 1500	> 1500	
	MTTR	hour	< 31	< 31	

11.4 Overlay

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Optical		Yes	Yes	
Process Targets	Overlay Control (3σ)	nm	6.4	4.4	
	Total Measurement Uncertainty (TMU) (3σ)	nm	< **1**	< 0.4	**22 nm requirement for DP**
	Tool Induced Shift (TIS) (3σ)		< 0.8	< 0.	
	Matching (mean)		< 0.4	< 0.4	
	Matching (site by site)		< 1.4	< 1.4	
	Pattern recognition failure rate (all layers)	%	< 0.05	< 0.05	
	Precison/Tolerance ratio	%	< 10	< 10	
Process Characteristics	Overlay Accuracy (mean) to be within total uncertainty of standard		to be measured	to be measured	
Defects, PWP @ 1.5 mm **edge exclusion target review with Suppliers – not final**	On bare Si ≥ 30 nm	#/cm^2	< 0.0021	< 0.0015	
	Backside on Si	#/cm^2	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	98	98	
	MTBF	Hour	> 1000	> 1000	
	MTTR	Hour	**< 2**	**< 2**	**Current capability**

General:

- Need to know 450 mm productivity requirements **(Coming in next Rev.)**
- Tool global requirements should be presented at the next workshop
- Wafer to wafer; chamber to chamber variability requirements is needed.
- Contamination measurement method and metrology, need to define a common agreeable method.

Comments:

- Better in San Jose then Austin – less travel, would like to see future ones either in San Jose or in Japan.
- Travel budgets shrinking – Flying support next meeting may not happen.
    - Web Ex discussion for metrics only might be ok, but other parts wouldn't be good for Web so prefer to keep it face to face.
- How can we do EPM better? Ask questions, but don't get follow up until after and get answers by email of less value because no follow up discussion.
    - Suggest to get supplier response to EPMs ahead of workshop and use workshop to provide the answers and further discussion.
- CMP – no technology show stoppers seen today. Takes time and resources.

Scaling of equipment: Throughput vs. footprint tradeoff is not straightforward in many equipment areas such as CVD, CMP, and area based.

- Strategic issue of addressing scaling issue vs. technology risk.
- Many target possible, but will need some CIP improvement and trade of tool size vs. productivity.

Scaling smartly vs. redesign decision is big challenge for suppliers. Taking risk on new tool types may result in better cost, but may not be accepted. How can suppliers get a better feel for how to manage risk?