450 mm Equipment Performance Metrics

ISMI Response after First Supplier Workshop

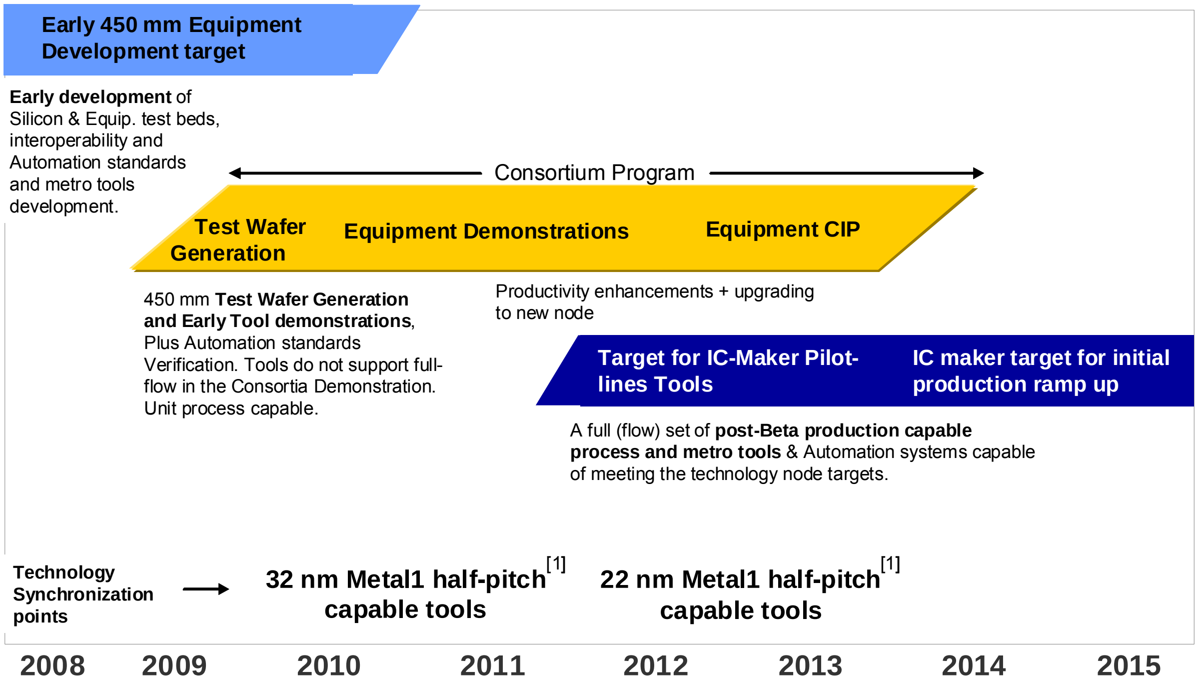
Purpose

This document conveys the customer expectations for process and manufacturing performance to Suppliers as they begin development of 450 mm equipment and look forward to the launch of manufacturing on the larger wafer size. In its initial release, the requirements focus on those tools identified by customers as highest priority for Supplier engagement; subsequent updates will encompass all wafer fab tools.

Introduction

IC Makers wish to work with Suppliers of wafer fab equipment to achieve capability for pilot lines in 2012 and prepare for manufacturing their products on 450 mm wafers. They have determined that their technology targets for the period coincide quite well with ITRS definitions for contacted metal half pitch at the 32 nm and 22 nm generations.

- The development and demonstration phase, roughly from 2010 to 2012, will focus on 32 nm capability from early testing to first production-worthy process and metrology equipment.
- Equipment maturation thereafter must achieve High Volume Manufacturing (HVM) cost/performance to support production ramp while technology scales to 22 nm and beyond.



Note: Detailed technology goals will be defined by individual company business requirements

[1]: Reference is DRAM stagger-contacted Metal 1 half-pitch in nanometers

Contents

I. Applicable Guidelines and Standards

The expectations for 450 mm tools include capabilities and configurations specified in the ISMI Unified 450 mm / Next Generation Factory Guidelines. Included are compliance with SEMI standards currently applicable to 300 mm tools or their equivalents for 450 mm, which may be under development at inception.

- Key is compliance with S2 Safety and S8 Ergonomics standards
- Other examples include the use of 25 Front Opening Unified Pods with 10 mm slot pitch as the in-fab carrier and the BOLTS standard for interface between E15.1 load ports and Equipment Front End Modules.

In addition, certain improvements, e.g. to FOUP purging and sealing capability, or the extension of standardization to platform / module interfaces may be developed.

The Guidelines, citing applicable standards, are included in these requirements by reference, and may be accessed at www.ismi.sematech.org, and SEMI Standards may be accessed at www.semi.org.

II. General Requirements

The overarching requirement for 450 mm manufacturing is that it maintain the advantageous cost structure that has enabled continuing growth for industry. While no explicit cost metrics are included in this document, this fundamental objective must be recognized in developing 450 mm equipment. The implications of this imperative are significant for all equipment, but for some types, specific elements will be called out in the individual metrics sheet.

A boundary condition is that 450 mm equipment be more productive than its 300 mm predecessor.

- For most equipment the ITRS Factory Integration requirement that productivity improve by 4% per year should be applied to the 300 mm 2009 baseline throughput in wafers per hour for the same tool configuration.
- It is recognized that for area-based tools, such performance will require major innovation and may not be achieved at the first generation; specific metrics and progress rates will be listed for such tool types.

450 mm manufacturing capability must comprehend the re-use of existing 300 mm facilities. The footprints of tools must not increase by more than 10% for a given number of wafers per unit time; the absolute heights of all process and metrology tools must be less than or equal to 12 feet.

Consumables represent a significant cost in manufacturing for many process steps. In general, consumables should be held to the same level for 450 mm as for 300 mm on a per-wafer basis. For some processes, significant reductions are required and will be specified in the individual metrics sheets.

ESH requirements are, broadly, to maintain or reduce the amounts of effluents and the use rates for most chemicals for 450 mm tools relative to the 300 mm 2009 baseline on a per-wafer basis.

- ***It is an absolute requirement that all equipment must be safe to operate and maintain at any stage of maturity.***
- ***Equipment spare parts and modules must either be small and light enough to handle safely during maintenance, and clearances adequate, or ergonomic handling aids must be provided.***

Personal Guided Vehicles (PGVs) will be required at inception for FOUP transport and for loading and unloading of FOUPS on tools.

III. Equipment Performance Metrics by Tool Type

450 mm Process and Metrology Equipment is categorized in the following one-page format by Tool Types, with sections for tool parameters, standards compliance and metrics for example processes and manufacturing performance.

Tool Types

Tool No.	Tool Type	Tool Description	Process Example
Lithography			
1.1	Exposure	193 nm	Critical levels
1.2	Exposure	193 nm Immersion	Critical levels
1.3	Exposure	248 nm	Non-critical levels
1.4	Track	Coat/develop	All levels
CMP			
2.1	CMP	Dielectric	Contact - Planarize PSG
2.2	CMP	Metal	(1) Contact - Tungsten Plug Polish
2.3	CMP		(2) Damascene - Copper Polish

CVD			
3.1	CVD	PECVD (HPCVD or HARP)	(1) Active Area - STI Fill - Undoped Ox
3.2	CVD		(2) SiN, SiCN Barrier / Etch Stop / Cap
3.3	CVD		(3) Low k Dielectric
3.4	CVD		(4) Contact - Nitride Etch Stop & Liner
3.5	CVD	Metal CVD	(1) Contact - Tungsten Plug
3.6	CVD		(2) Contact - Ti/TiN Barrier for W Plug
3.7	CVD		(3) TaN Barrier for Cu Metal layers
3.8	CVD		(4) TiN Metal Hard Mask for Damascene Etch
3.9	CVD	ALD	High k, Tungsten; SiGe
PVD			
4.1	PVD	PVD-Metal	(1) Gate Metal
4.2	PVD		(2) Silicide Metal
4.3	PVD		(3) Cu Seed
4.4	PVD	Reactive Sputter	(1) Contact - Ti/TiN Barrier for W Plug
4.5	PVD		(2) TaN Barrier for Cu Metal Layers
4.6	PVD		(3) TiN Metal Hard Mask for Damascene Etch
Dry Etch			
5.1	Dry Etch	Dielectric; Poly	Active Area - STI Trench
5.2	Dry Etch	Dielectric	(1) Gate - Nitride Spacer
5.3	Dry Etch		(2) Contact
5.4	Dry Etch		(3) Via / Damascene Trench
5.5	Dry Etch	Poly	Gate - Polysilicon / ARC
5.6	Dry Etch	Metal	(1) Gate - Metal Electrode
5.7	Dry Etch		(2) Silicide Metal
5.8	Dry Etch		(3) Metal Hard Mask for Damascene
Dry Strip			
6.1	Dry Strip	Asher	(1) Active Area
6.2	Dry Strip		(2) Source/Drain Implant
6.3	Dry Strip		(3) Gate Electrode, Silicide, Metal Hard Mask
6.4	Dry Strip	Bevel clean	Wafer Edge
Electrochemical Plating			
7.1	Electrochemical Plating	Copper	Damascene Fill
Doping			
8.1	Ion Implantation	High Energy	Deep Wells
8.2	Ion Implantation	Medium Current	Gate Extensions
8.3	Implant / Plasma Immersion	Low Energy / High Current	Source / Drain
Thermal Process			
9.1	Thermal Process	Oxidation Vertical Furnace	(1) Active area- Field Oxide
9.2	Thermal Process		(2) Rounding oxidation
9.3	Thermal Process		(3) N-well Sacrificial Oxide
9.4	Thermal Process	Anneal Vertical Furnace	(1) Densification
9.5	Thermal Process		(2) Low Temp Anneal
9.6	Thermal Process	Nitride LPCVD	Gate Spacer
9.7	Thermal Process	Poly LPCVD	Gate Electrode
9.8	Thermal Process	Rapid Thermal Anneal	(1) Silicide
9.9	Thermal Process		(2) Source / Drain Anneal
Wet Process (Single Wafer or Batch Process?)			
10.1	Wet Etch	Wet Nitride	Active-area- Oxy-Nitride Strip
10.2	Wet Clean	VP-HF	Active area- Ozone/Anhydrous HF clean
10.3	Wet Clean	Wet Clean	(1) Particle Removal
10.4	Wet Clean		(2) Pre- / Post-Ash
10.5	Wet Clean		(3) Backside Clean
10.6	Wet Clean	Solvent	Solvent Clean
Metrology			
11.1	Bare Wafer Particle		
11.2	Film Thickness		
11.3	CD		
11.4	Overlay		
11.5	Patterned Defect		

How to View the Following Requirements

Each metric is listed by attribute with units and targets for 32 nm and 22nm. Suppliers should target 32 nm capabilities by the 2010-11 demonstration period and plan for extension to 22 nm capability by the 2012-14 piloting phase. Manufacturing metrics are expectations for HVM.

It is recognized that, initially, tools will not be as capable with regard to either process or productivity goals as the metrics presented in this document, and may not comply with all guidelines and standards. They must be safe to operate and maintain.

> To support early development of equipment in 2009 - 2010, certain tools will be required to provide test wafer capability before they are mature enough for demonstration. There are relaxed expectations for their performance at inception and key parameters will be specified through consultation with Suppliers for this starting phase.
>
> > ***A separate document will detail these less-stringent expectations of tools needed early for test wafer generation.***
>
> Performance improvement for test wafer generation must be pursued in parallel as the overall capability of the tools is developed. The expectations for performance during demonstration and production launch for all tools, including those needed at early maturity for test wafer generation, will be included in this document as it is developed in consultation with Suppliers.

A separate document encompassing Demonstration Test Methods will detail the means to scale targets accouning for equipment maturity and determine statistical sampling for required confidence, as well as the test structures to be used in demonstration testing.

Contact Information

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Metrics Definitions

Equipment name – This identifies the equipment type and specific process application, key process parameters, sampling plan, etc.

Equipment parameters – This identifies desired unique equipment features like stepper/scanner field size, electrostatic chuck for vacuum tool applications, integrated or clustered tools, etc.

Throughput – Raw throughput in wafers per hour assuming 100% uptime (continuous, uninterrupted processing, cascade mode, and not depreciated for downtime, setup, etc.). For metrology tools, throughput may be weighted by a sampling plan if specified on the equipment metrics form.

Mean Time Between Failure (MTBF) – Mean productive time to fail as a function of processing time, not clock time. This definition is in line with the SEMI E10-0304 standard.

Mean Time To Repair (MTTR) – This includes qualification test time. This definition is in line with the SEMI E10 standard.

Edge exclusion – Area around the wafer edge that does not receive uniform/reliable processing and will not yield complete electrical circuit.

Note: For purposes of this document, a 1.5 mm edge exclusion is expected.

Defectivity – *represented by the particle density above a referenced threshold defect size outside the edge exclusion zone.*

- Defect Density is number of particles per unit area, typically per square centimeter.
- PWP - Per Wafer Pass refers to the particles added to the wafer by one cycle through the tool / process.
- For purposes of this document and the early demonstrations of 450 mm equipment, bare wafer defect levels are converted to equivalent density at 30 nm particle size to reflect current detection capability.
    - For reference, if 50 nm defect detection is used, target is adjusted to 40% of the number listed for bare wafer at 30 nm in the metrics sheet.
- Defectivity metrics for each tool may include targets for bare wafer, back side, in-film and/or with-pattern particle densities, as applicable

Process – This is a ***generic*** process that highlights key process criteria for each tool. It is used to develop tool performance data as outlined above and is also intended to be used for 450 mm equipment performance demonstrations. Processes will essentially be the same as for 300 mm.

Factory and Equipment Performance Metrics

Numbering for factory and equipment tables.

Appendix	Revision	Description
1		Lithography
2		CMP
3		CVD
4		PVD
5		Dry Etch
6		Dry Strip
7		Electrochemical Plating
8		Doping
9		Thermal Process
10		Wet Process
11		Metrology
		(future) Personal Guided Vehicle (PGV)
		(future) Load Port/EFEM
		(future) Carriers
		(future) AMHS
		(future) ESH
		(future) Stocker
		(future) Equipment Software
		(future) Factory Automation Software
		(future) FOUP Cleaner
		(future) Wafer Sorter

Document Revision History

Revision	Appendix Revised	Date	Reason For Change
Initial Release		11/18/08	
1.0	All	12/30/08	ISMI Response to 11/18/08 Supplier Workshop

First Ten Tools for ISMI Demonstrations

Initial focus of Intel, Samsung and tsmc

Metrics for Demo and Production in this Revision

193 nm Scanner / Lithography Track
PECVD Dielectric
Dielectric CMP
PVD Metal
Dielectric Dry Etch
Electrochemical Cu Plating
High Energy Ion Implant
LPCVD Silicon Nitride
Wet Cleans
Bare Wafer Particle Detection

Tools Needed Early for Test Wafer Generation

Relaxed Initial Expectations in Separate Document

Early Patterning Capability
Oxide Vertical Furnace
PECVD Dielectric
Dielectric Dry Etch
Dielectric CMP
PVD Metal
LPCVD Nitride
Wet Cleans
Dry Strip Asher
Bare Wafer Particle Detection
Thin Film Thickness
CD Measurement

Appendix 1 – Lithography

1.1 Exposure, 193 nm, Critical levels (tsmc needs Immersion @ 22 nm)

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Min. field size (6 inch reticle)	mm x mm	26 x 33	26 x 33	
	Reduction	Ratio	4:1	4:1	
	Reticle size (6 inch reticle)	inch x inch	6 x 6	6 x 6	
	Partial die at wafer edge		patterned	patterned	
Process Targets	CD Nominal	nm	32	23	
	CD Control (3σ)	nm	< 2.6	Intra<1.0; Inter <1.0	At best focus / best dose; wafer flatness will be specified for demo
	Total overlay, tool to tool, compatibility	nm	< 6.4	< 4	Ave. + 3σ
	Overlay to self	nm	< 3	< 2	May need to be tighter for double patterning
	Dynamic depth of focus, full field ± CD Control	nm	> 150	> 150	
	Resist-sensitivity typical	mJ/Cm^2	20–50 mJ/ cm2	20–50 mJ/ cm2	
	Ref. exposure energy	mJ/Cm^2	25	25	
Process Characteristics	Evaluation pattern (1) Line / Space	nm	32	23	CD after develop / bake (no trimming)
	Evaluation pattern (2) Isolated Line	nm	21	15	Likely to require double patterning
	Throughput vs. exposure energy	wafer/hr	to be measured	to be measured	Range of doses to to be specified
	Setup time per recipe	Min	to be measured	to be measured	
	CD repeatability across the wafer, multi-width	nm	to be measured	to be measured	
	Overlap DOF parameters	µm	to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0022	< 0.0007	
	Backside on Si	$\#/cm^2$	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	

Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required*
	Availability	%	96	96	Bottleneck tool
	MTBF	Hour	> 700	> 700	
	MTTR	Hour	< 29	< 12	

It is recognized that the throughput requirements shown here are aggressive and will require significant design enhancements.

As was the case at 300 mm, productivity improvements are expected to be introduced over the first couple of 450 mm tool generations

Appendix 1 – Lithography

1.4 Track, Coat/Develop

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	ARC		yes	yes	
	Edge bead removal (EBR)		yes	yes	
Process Targets	Process resist thickness	nm	50 - 90	35 - 65	
	Coating uniformity total variability (3 σ)	nm	< 2.1	< 2.1	
	Coating uniformity within wafer (3 σ)	nm	< 1.5	< 1.5	
	Coating uniformity wafer to wafer (3 σ)	nm	< 1.5	< 1.5	
	Develop uniformity within wafer (3 σ)	nm	< 5	< 5	
	Develop uniformity total variability (3 σ)	nm	< 4	< 4	
	Develop uniformity wafer to wafer (3 σ)	nm	< 3	< 3	
	Bake uniformity total variability (90–110°C) (3 σ)	°C	< 0.2	< 0.2	
	Bake uniformity total variability (110–150°C) (3 σ)	°C	< 0.3	< 0.3	
	EBR D Radius (3 σ)	mm	< 0.15	< 0.15	
	Photo resist Dispense volume (for saving)	cc/wfr	< 1.0	< 1.0	Needs more evaluation
Process Characteristics	Contact angle after adhesion process	Degree	60–70	60–70	
	NH3 concentration	Ppb	< 1.0	< 1.0	
	EBR D Theta (3 σ) (Optical EBR/Notch Area)	Degree	to be measured	to be measured	
	Life of chemical filter in 50 ppb cleanroom	Months	> 12	> 12	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0013	< 0.001	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
	Pattern	#/cm^2	< 0.02 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Must not limit scanner	Must not limit scanner	
	Availability	%	96	96	
	MTBF	Hour	> 700	> 700	Bottleneck tool
	MTTR	Hour	< 29	< 24	
	Wafer transfer failure rate (transfer reliability)			< 1/1000	

Appendix 2 – CMP

2.1 CMP, Dielectric, Contact – Planarize PSG

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto pad condition		required	required	
	In situ thickness monitor and control/endpoint cntl		required	required	APC/EPD required
	APC		required	required	Host communicate incoming uniformity and compensation parameters
	Integration with post – CMP clean		required	required	
	Dry in – Dry out		required	required	
Process Targets	CMP uniformity total variability (3 σ) – all sources	%	< 10	< 5	
	Head-to-head variation in removal rate (3 σ)	%	< 3	< 1.5	
	Dielectric thinning (condition: over-polish 15%)	nm	tbd	tbd	Structure to be specified for demo
Process Characteristics	Rate stability parameters (drift, pad life >500 wafers)	%	< 10	< 5	Must compensate for pad life
	Scratches	$/cm^2$	< 0.1	< 0.1	
	Removal rate	nm/min	500	500	
	Dishing/over/under erosion on patterned wafers	nm	to be measured	to be measured	
	Slurry Waste	lpm	Per wafer, same as 300 mm or better	Per wafer, same as 300 mm or better*	
	Pad Consumption		TBD	TBD*	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0050	< 0.0076	.
	Backside on Si	$\#/cm^2$	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	

Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability MTBF MTTR	% Hour Hour	95 > 400 < 21	95 > 400 < 21	

* CMP is one of the key processes where consummables cost must be brought down significantly, either with new designs for 450 mm or engineering improvements over time

Appendix 3 – CVD

3.1 CVD, PECVD - STI Fill / Undoped Ox

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness	nm	350	350	Process specific
	Film thickness uniformity total variability (3 σ)	%	< 3	< 3	Thickness dependent
	Stress (compressive)	Mpa	> 150 and < 250	> 150 and < 250	Process specific
Process Characteristics	Film shrinkage	%	to be measured	to be measured	
	Step coverage	%	95	95	
	Metal contamination	atm/cm²	< 1E10	< 1E10	
	Refractive Index (RI)		to be measured	to be measured	
	Plasma charge damage		to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0068	< 0.0042	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 500	> 500	
	MTTR	Hour	< 26	< 26	

Appendix 4– PVD

4.3 PVD, Sputter for Cu Barrier/Seed

Note: these films may require processes other than PVD to achieve required conformality at 32 nm and 22 nm.

We will provide additional guidance as development proceeds

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Comments
Equipment Parameters	Wafer temperature range	°C	25–500	25–500	
	Base vacuum @ 250°C	Torr	< 1.00 E-8	< 1.00 E-8	
	Pre clean function required		yes	yes	
Process Targets	Ti thickness	nm	20	20	
	Al 0.5% Cu thickness	nm	400	400	
	TiN thickness	nm	25	25	
	Pre clean oxide etch uniformity total variability (3 σ)	%	< 3	< 3	< 2
	Film thickness uniformity total variaiblity (3 σ)	%	< 3	< 3	<2
	Ti/TiN bottom coverage (logic)	%	> 20	> 20	
	Pre clean charge up damage		None	None	None
Process Characteristics	Ti resistivity	μW – cm	to be measured	to be measured	
	Ti stress	Pa	< 1.00E+9	< 1.00E+9	
	TiN stress	Pa	to be measured	to be measured	
	AlCu resistivity	μW – cm	< 1.00E+9	< 1.00E+9	
	Sidewall coverage parameters	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0047	< 0.0034	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	96	96	
	MTBF	hour	> 700	> 700	
	MTTR	hour	< 4	< 4	

Appendix 5 – Dry Etch

5.3 Dry Etch, Dielectric, Contact

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto End-point Detection	-	Required	Required	
	in-situ Bevel Defect Detection		Required	Required	Need better solution to eliminate bevel polymer contamination
	In-situ Chamber Clean	-	Required	Required	
Process Targets	Contact CD at Resist	nm	39	28	
	Contact CD after Etch	nm	36	25	
	Aspect Ratio	H:D	> 10:1	> 14:1	Relaxed from 20 and 30
	Total Variability 3σ – all sources	nm	< 1.5	< 1	
Process Characteristics	Selectivity to	-	> TBD , each company input selectivity requirements w.r.t materials chosen	> TBD, each company input selectivity requirements w.r.t materials chosen	
	Loading Effect	%	< 5	< 5	Etch rate difference l/s to iso
	Charge Damage	-	To be measured	To be measured	
	Residue after etch	-	None	None	
	Metal contamination	Atoms /cm^{-2}	1E10	1E10	See Note at end
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0084	< 0.0060	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	Need to find better solution for e-chuck to eliminate need for post-etch backside clean
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 350	> 350	
	MTTR	hour	< 18	< 3	
	MTB/T Clean		To be measured	To be measured	Will depend on process chemistry

Appendix 6 – Dry Strip

6.1 Dry Photoresist Strip, Asher

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Auto endpoint		Required	Required	
	Wafer temperature controller		Required	Required	
Process Targets	Ashing rate	µm/min	> 10	> 10	
	Ashing rate uniformity within wafer (3 σ)	%	< 5	< 5	
	Ashing rate uniformity wafer to wafer (3 σ)	%	< 5	< 5	
	Selectivity to all but resist	Ratio	> 500	> 500	
	Oxide loss (implanted)	Nm	< 0.1	< 0.1	
	Silicon loss	Nm	< 0.1	< 0.1	
Process Characteristics	Charge up damage		None	None	
	Metallic contamination	atms/cm^2	1.00E+10	1.00E+10	See Note at end
	CV shift	mV	to be measured	to be measured	Process dependent
	Residue after ashing detectable by dark field microscope or defect tool haze indication		None	None	
	Temperature control to	deg – C	350 +/- 10	350 +/- 10	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0028	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	Hour	> 900	> 900	
	MTTR	Hour	< 47	<3	

Appendix 7 – Electrochemical Plating

7.1 Cu Plating (700 nm Cu Film)

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness total variability (3 σ)	%	< 3	< 3	
	Resistivity	μOhm-cm	< 1.8	< 1.8	< 1.8μ Ω -- cm @ 1μ m (anneal@100C,60min)
	Trench size/via size	nm	43 / 36	30 / 25	
	Contact fill (single damascene at < 40 nm trench)	aspect ratio	6	6	Relaxed from 20
Process Characteristics	Film stress		to be measured	to be measured	< 120MPa @ 1μ m
	Void formation		Free	Free	
	Grain size		to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0021	< 0.0015	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	>500	>500	
	MTTR	hour	< 4	< 4	

Appendix 8 – Doping

8.1 Ion Implantation: High Energy

.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment mechanical wafer throughput	wafer/hr	230	230	
Process Targets	Energy range Max (single charge)	keV	3000	3000	
	Energy range Min (single charge)	keV	10	10	
	Dose range Max	Ion/cm^2	1.00E+15	1.00E+15	
	Dose range Min	Ion/cm^2	1.00E+10	1.00E+10	
	Dose uniformity total variability (3 σ)	%	< 1.3	< 1.3	
	Dose uniformity within wafer (3 σ)	%	< 1.3	< 1.3	
	Dose uniformity wafer to wafer (3 σ)	%	< 1.3	< 1.3	
	Dose repeatability total variability (3 σ)	%	2	2	
	wafer to wafer (3 σ)	%	1.3	1.3	
	Dose repeatability within wafer (3 σ)	%	1.3	1.3	
	Mass resolution	M/DM	> 60	> 60	
Process Characteristics	Metallic contamination (Cr, Fe, Co, Ni, Zn, Mn, Ti)	atm/cm^2	1.00E+10	1.00E+10	
	Metallic contamination (Na, K, Mg, Ca, Al, Cu, Au, Ag)	atm/cm^2	5.00E+09	5.00E+09	
	Dose purity parameters measured (SIMS)	%	< 0.5	< 0.5	
	Cross contamination	%	< 0.1	< 0.1	
	Beam current parameters		to be measured	to be measured	
	Beam set-up: solid source (hot start)	min	< 10	< 4	
	Wafer temperature As+, maximum beam current	°C	60	60	
	Beam stability glitch 5 keV ~ max energy	#/ hour	< 5	< 5	
	Beam stability fluctuation 5 keV ~ max energy	%	< ± 5	< ± 1	
	Beam stability parallelism 5 keV ~ max energy	%	to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0027	< 0.0020	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	

Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	Innovation required
	Availability	%	96	96	Bottleneck tool
	MTBF	hour	> 250	> 250	
	MTTR	hour	< 10	< 10	

Appendix 9 – Thermal Process

For thermal processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

9.1 Thermal Process, Oxidation Vertical Furnace

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Target oxide thickness	nm	45	45	
	Oxide thickness uniformity total variability (3 σ)	%	2	2	
Process Characteristics	Metallic contamination (Cr, Fe, Co, Ni, Zn, Mn, Ti)	atm/cm^2	1E10	1E10	
	Metallic contamination (Na, K, Mg, Ca, Al, Cu, Au, Ag)	atm/cm^2	5E9	5E9	
	Slip-free process at maximum temperature	°C	950	950	
	Residual oxygen concentration (400–1000°C)	ppb	To be measured	To be measured	See note below
	Spontaneous oxide thickness (400°C, N2)	nm	To be measured	To be measured	See note below
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0022	< 0.0016	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 52	< 4	

Note: Oxygen concentration will be measured in the process chamber under purge conditions through this temperature range; thickness of any oxide grown on a bare Si wafer pushed and pulled under these conditions will be measured

9.6 Thermal Process, Nitride LPCVD, Gate Spacer

For thermal processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters					
Process Targets	Film thickness	nm	40	35	
	Total variability (3 sigma)	%	< + 2	< + 2	
	Step Coverage	%	> 90	> 90	
	Process Temperature	deg-C	< 400	< 400	Conformal
	Pattern Loading Effect	%	< 5	< 5	Difference l/s to iso
Process Characteristics	Stress (as deposited)	MPa	< 100	< 100	Structure to be specified for demo
	Metallic contamination	atoms / cm^2	< 1E10	< 1E10	See Note at end
	Refractive index / variability		To be measured	To be measured	
	Supplier specify process to achieve film				
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0028	
	In-film	#/cm^2	< 0.01 @ ≥ 20 nm	< 0.01 @ ≥ 10 nm	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 300	> 300	
	MTTR	hour	< 16	< 4	

Appendix 10 – Wet Processes

For wet cleans processing, key equipment metrics are productivity and and cost of ownership.
Equipment suppliers should optimize their equipment designs (single wafer vs. batch) based on these goals.

10.3 Wet Cleans, Particle Removal

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	IPA drying		yes	Yes	
	HF temperature control (ambient)	°C	< ± 0.2	< ± 0.2	
	SCx temperature control (22-80°C)	°C	< ± 0.5	< ± 0.5	
	HF Chemical concentration control	%Wt	< ± 2	< ± 1	
	SCx Chemical concentration control	%Wt	< ± 5	< ± 2	
Process Targets	HF etch uniformity total variability (3σ)	%	< 2.5	< 1.5	
	0.17 µm Particle Removal Efficiency (Si_3N_4) (particles added by dipping, limit is 1,000~10,000)	%	> 95	> 95	
	Water marks (HF last)	count	none	None	
	Pattern Damage	count	none	none	Test structure to be defined for demo
	Silicon Loss per Clean Pass	Ang	0.3 Ang	0.2	
	Particle Removal Efficiency (PRE) on bare wafer	%	90% ≥ 30 nm	90% ≥ 30 nm	Nitride particle on Oxide surface
	PRE with no pattern damage on wafer with 30 nm trench		70%	70%	
	Backside Clean Efficiency	%	85% ≥ 65 nm	85% ≥ 65 nm	
	Residue after SPM/APM detectable by dark field microscope or defect tool haze indication		None	None	
Process Characteristics	Metallic contamination (Cr, Fe, Co, Ni, Zn, Mn, Ti)	atm/cm²	< 1E10	< 1E10	
	Metallic contamination (Na, K, Mg, Ca, Al, Cu, Au, Ag)	atm/cm²	< 2E9	< 2E9	

	Breakdown Voltage	V	to be measured	to be measured	Process specific
	TDDB	sec	to be measured	to be measured	Process specific
	Process time reproducibility (10 runs 3σ)	sec	< 1	< 1	Process time only
	Wafer transport time reproducibility (10 runs 3σ)	sec	< 1	< 1	Batch tool robotic element
	Time for exchange of chemical in bath	min	< 1.5	< 1.5	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0038	< 0.0027	
	Backside on Si	#/cm^2	< 0.28 @ ≥ 75 nm	< 0.28 @ ≥ 50 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	95	95	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 6	< 4	

Appendix 11 – Metrology

11.1 Bare Wafer Particle

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Equipment Integration with inspection SEM		capable	capable	
	Ability to mask prealignment laser marks		capable	capable	
	Automatic detect classification (in line binning)		capable	capable	
	Ability to perform map difference analysis		capable	capable	
	Communications software/networkability capability		capable	Capable	
Process Targets	Particle sensitivity @ 90% capture rate	nm	30	30	
	Defect size range	nm	30 - 10000	30 - 10000	
	Total count reproducibility (3 sigma) using 30 nm sphere at > 100 count	%	< 2	< 2	
	Coordinate accuracy (repeatability, 3 sigma)	µm	< 5	< 5	
	Absolute coordinate accuracy (newly added)	µm	< 10	< 10	
	Tool-to-tool matching	%	< 3	< 3	
	Precison to Tolerance (P/T) Ratio by size	%	< 15	< 15	
Process Characteristics	Haze sensitivity parameters	ppm	to be measured	to be measured	
	Haze to dynamic range relationship		to be measured	to be measured	
	Edge exclusion	mm	1.5	1.5	
Defects, PWP @ 1.5 nm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.003	< 0.0022	
	Backside on Si	#/cm^2	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Throughput	wafer/hr	Area-scaled equivalent to 300 mm + 50%	Wafer rate equivalent to 300 mm	
	Availability	%	98	98	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 20	< 20	

It is recognized that the throughput requirements shown here are aggressive and will require significant design enhancements.

As was the case at 300 mm, productivity improvements are expected to be introduced over the first couple of 450 mm tool generations

Appendix 11 – Metrology

11.2 Film Thickness

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameter	Ability to measure thickness, refractive index, & extinction coeff., reflectivity (RI @ 633, 248, 193 nm)		yes	Yes	
	Ability to measure film stack (RI @ 633, 248, 193 nm)		yes	Yes	
	Reproducibility (Total, 3 σ) site with pattern recognition and 30 µm x 30 µm test site without pattern recognition (RI @ 633, 248, 193 nm)		yes	Yes	
Process Targets	Coordinate accuracy allows "systematic coordinate information" (3σ)	µm	< 1.5	< 1.5	
	Tool to tool matching T, n, K (single layer) (1% total error budget) > 100A	%	< 0.5	< 0.5	
	Tool to tool matching < 100 A		0.2	0.1	
	For 25 nm gate oxide	%	< 0.05	< 0.05	
	Pattern recognition errors (all layers)	%	< 0.01	< 0.01	
	Thickness range (oxide)	Å	5–200 K	5–200 K	
	P/T T = ± 10% when mean thickness < 30 Å T = ± 5% when 30 Å < mean thickness < 1K Å T = ± 1% when 1K Å < mean thickness < 100K Å	%	<10	<10	
Process Characteristics	Accuracy (mean) to be within total uncertainty of standard (Oxide NIST sample)	nm	to be measured	to be measured	
	Result of 30 time repeated test:				
	Accuracy (mean value) : < 10 nm	Å	± 0.5	± 0.5	
	: < 1 µm	Å	± 1	± 1	
	Repeatability : < 10 nm	Å	0.2	0.2	
	: < 1 µm	Å	0.25	0.25	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	#/cm^2	< 0.0022	< 0.0016	
	Backside on Si	#/cm^2	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	98	98	
	MTBF	hour	> 1000	> 1000	
	MTTR	hour	< 20	< 20	

Appendix 11 – Metrology

11.3 CD

	Attribute	Units	Metrics (32 nm)	Metrics (22 nm)	Notes
Equipment Parameters	Automated SEM		yes	Yes	
Process Targets	CD range	nm	40–5000	40–5000	
	Cd tolerance (reference only) Si etching L/S pattern, 260 nm Pitch	nm	< 3	< 3	
	Reproducibility over one month (3 σ) Si etching L/S pattern, 130 nm Line and 260 nm Pitch	%	< 1.5	< 1.5	
	Pattern recognition failure rate (all layers)	%	< 0.05	< 0.05	
	Tool-to-tool matching Si etching L/S pattern, 130 nm Line	%	< 0.5	< 0.5	
	Process/Tolerance	%	< 20	< 20	
Process Characteristics	CD Accuracy (mean) to be within total uncertainty of standard		to be measured	to be measured	
	Charging effect over 30 seconds		to be measured	to be measured	
	Contamination effect after 50 measurements		to be measured	to be measured	
	Contact resolution (top and bottom) 150 nm and 180 nm		to be measured	to be measured	
Defects, PWP @ 1.5 mm edge exclusion	On bare Si ≥ 30 nm	$\#/cm^2$	< 0.0026	< 0.0019	
	Backside on Si	$\#/cm^2$	< 0.25 @ ≥ 160 nm	< 0.25 @ ≥ 110 nm	
Manufacturing Targets (@ High Volume Manufacturing Phase)	Availability	%	98	98	
	MTBF	hour	> 1500	> 1500	
	MTTR	hour	< 31	< 31	

Note on Metallic Contamination

Preliminary guidance - requirements may be changed for 32 nm and 22 nm as development proceeds

All metals should generally be present on wafer surfaces after processing at no more than 1E10 atoms per cm^2

Cr, Fe, Co, Ni, Zn, Mn, Ti are examples of metals for which contimination levels will be measured

Na, K, Mg, Ca, Al, Cu, Au, Ag have greater impact and tighter requirements specified in some tools